

RELIABILITY REPORT
FOR
MAX15157ATJ+T
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX15157ATJ+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX15157 fixed-frequency, current-mode PWM controller drives four power MOSFETs in an H-bridge configuration, allowing the regulator to operate as a stepdown and/or step-up regulator. When the input and output voltages are near each other, both control loops operate and the regulator switches all four power MOSFETs, accurately regulating the output voltage. The output voltage can be dynamically set through the 0.4V to 2.2V reference input (REFIN) for modular design support. The switching frequency is controlled either through an external resistor setting the internal oscillator frequency, or by synchronizing the regulator to an external clock. The device is designed to support 120kHz to 1000kHz switching frequencies. The controller has a dedicated input undervoltage-lockout input (UVLO) and an accurate enable-input threshold for flexible power-sequence configuration. The regulator also has multiple fault-protection circuits to protect against overcurrent, output overvoltage, output undervoltage, and thermal shutdown. These fault conditions will reset the regulator (hiccup) by resetting the soft-start capacitor and attempting to power up again using the soft-start sequence. The device is available in a 32-pin TQFN package and supports a -40°C to +125°C junction temperature range.

II. Manufacturing Information

A. Description/Function:	60V H-Bridge Step-Up/Down Controller
B. Process:	S18
C. Number of Device Transistors:	31902
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	September 25, 2014

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5715
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	107.874X107.874 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAWT4Q001B, D/C 1434)

The NS04-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX15157ATJ+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SAWT4Q001B, D/C 1434

Note 1: Life Test Data may represent plastic DIP qualification lots.