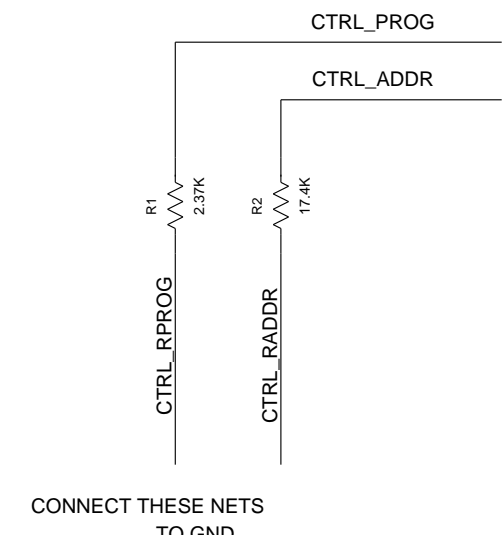
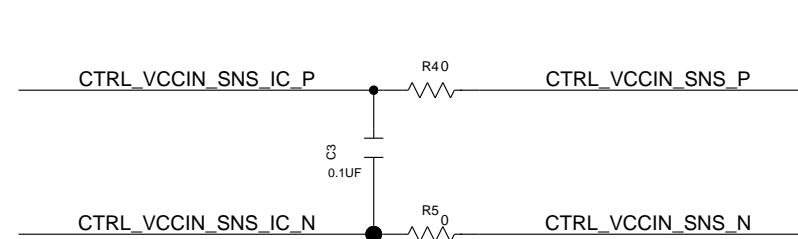


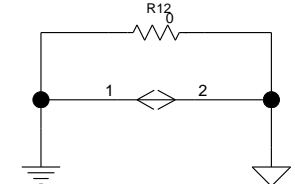
CONFIGURATION



HF POLE

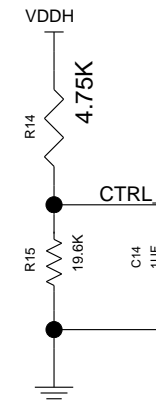


INTERNAL SW DISABLE

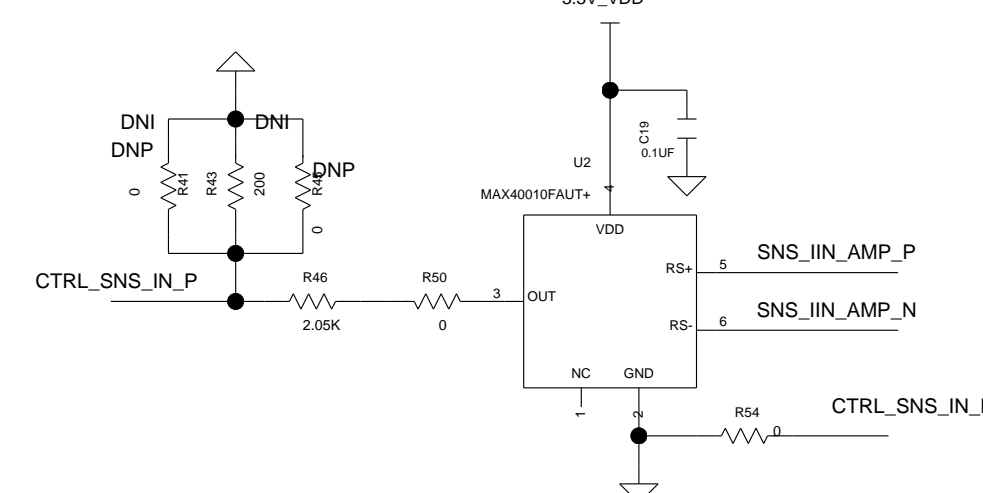


INSTALL TO DISABLE INTERNAL SWITCHER

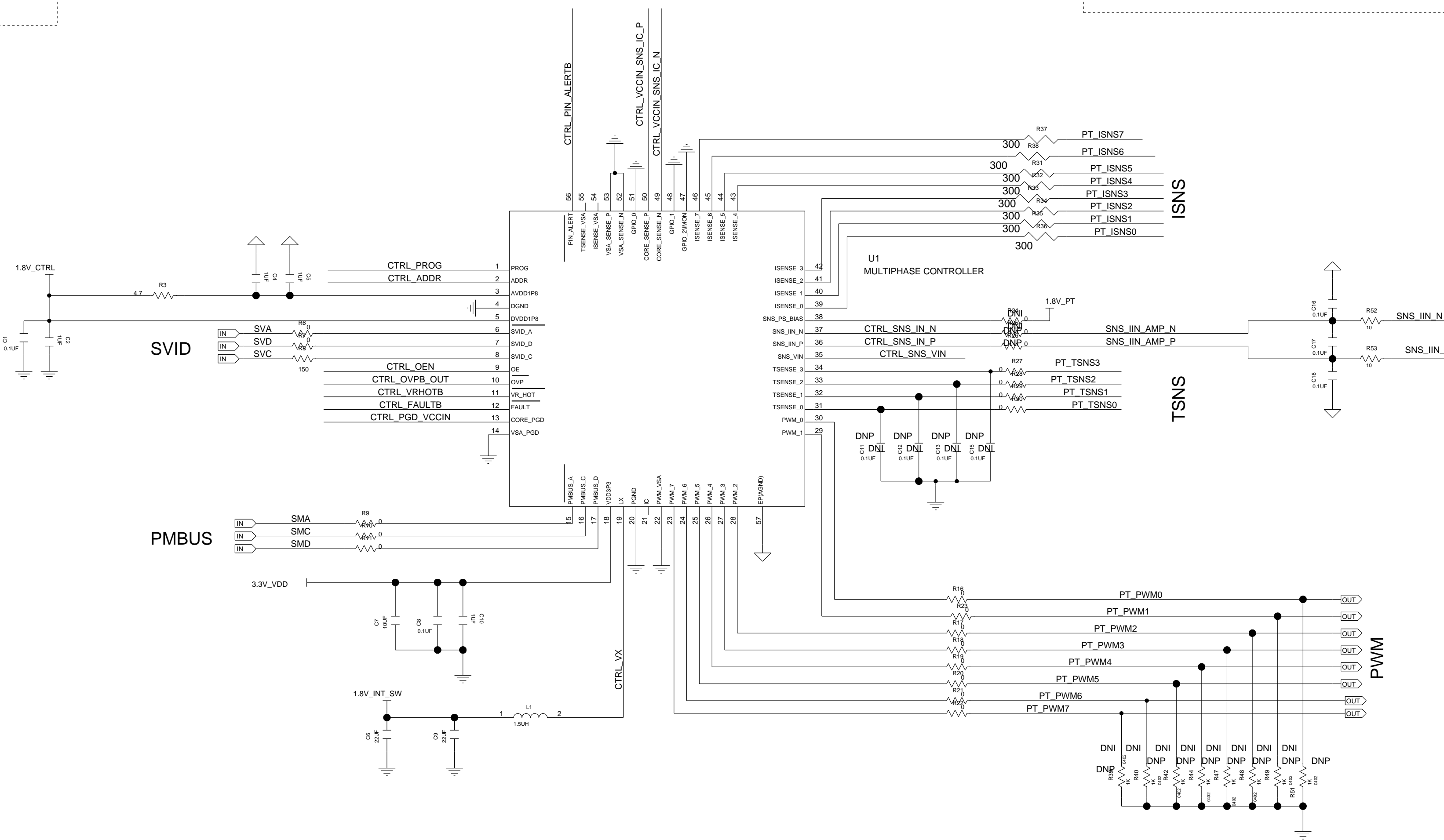
VIN SENSE



INPUT SNS AMPLIFIER

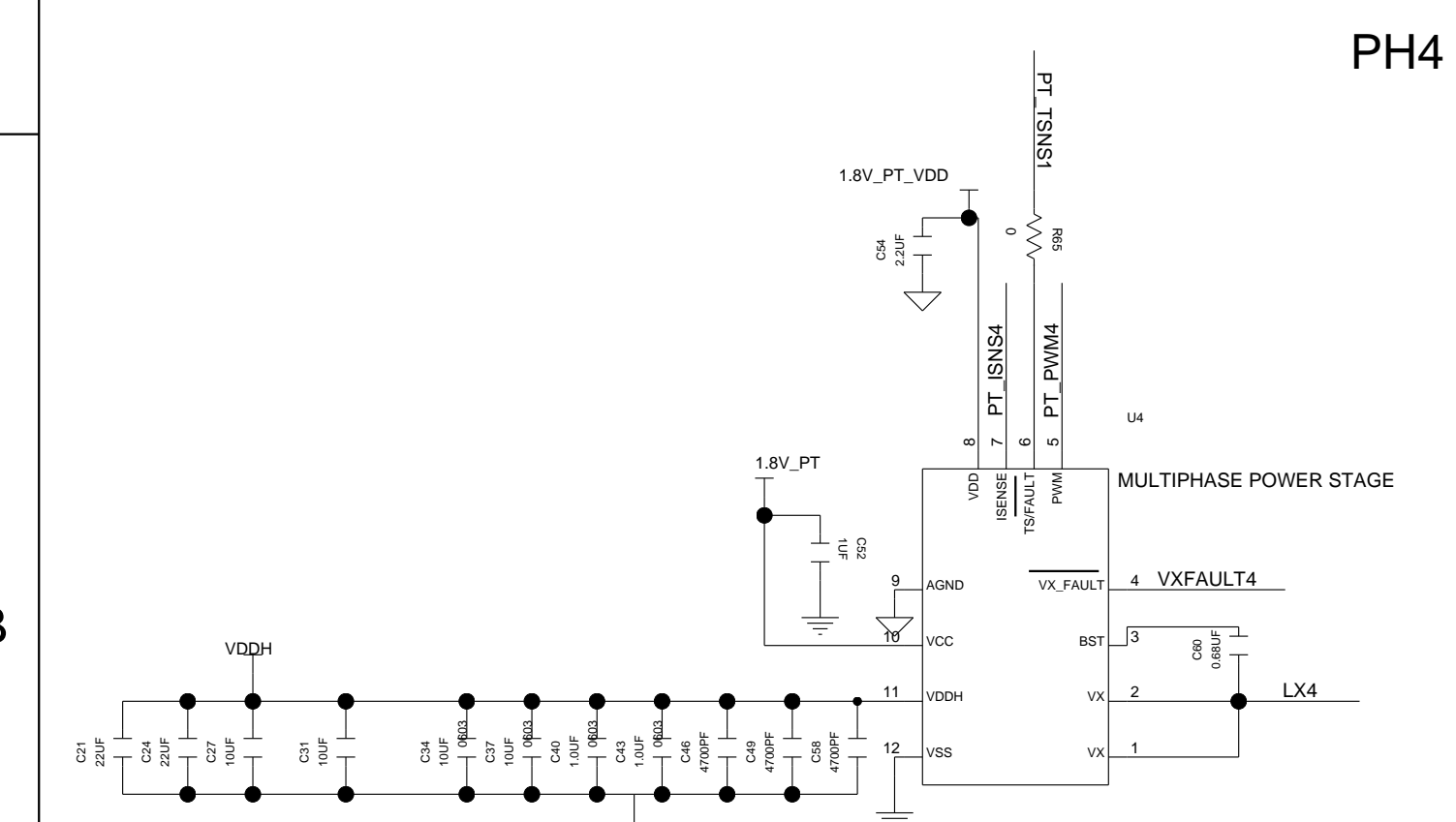
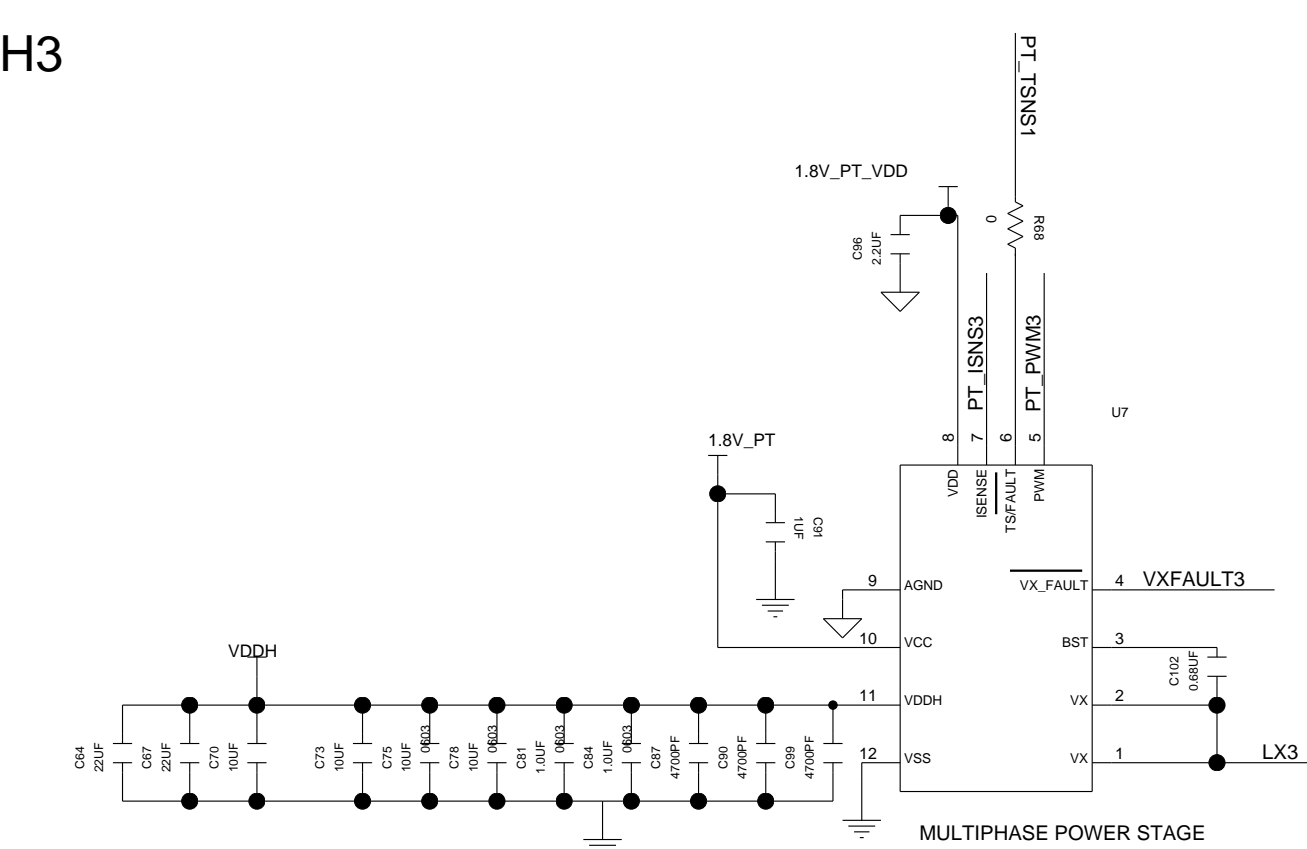
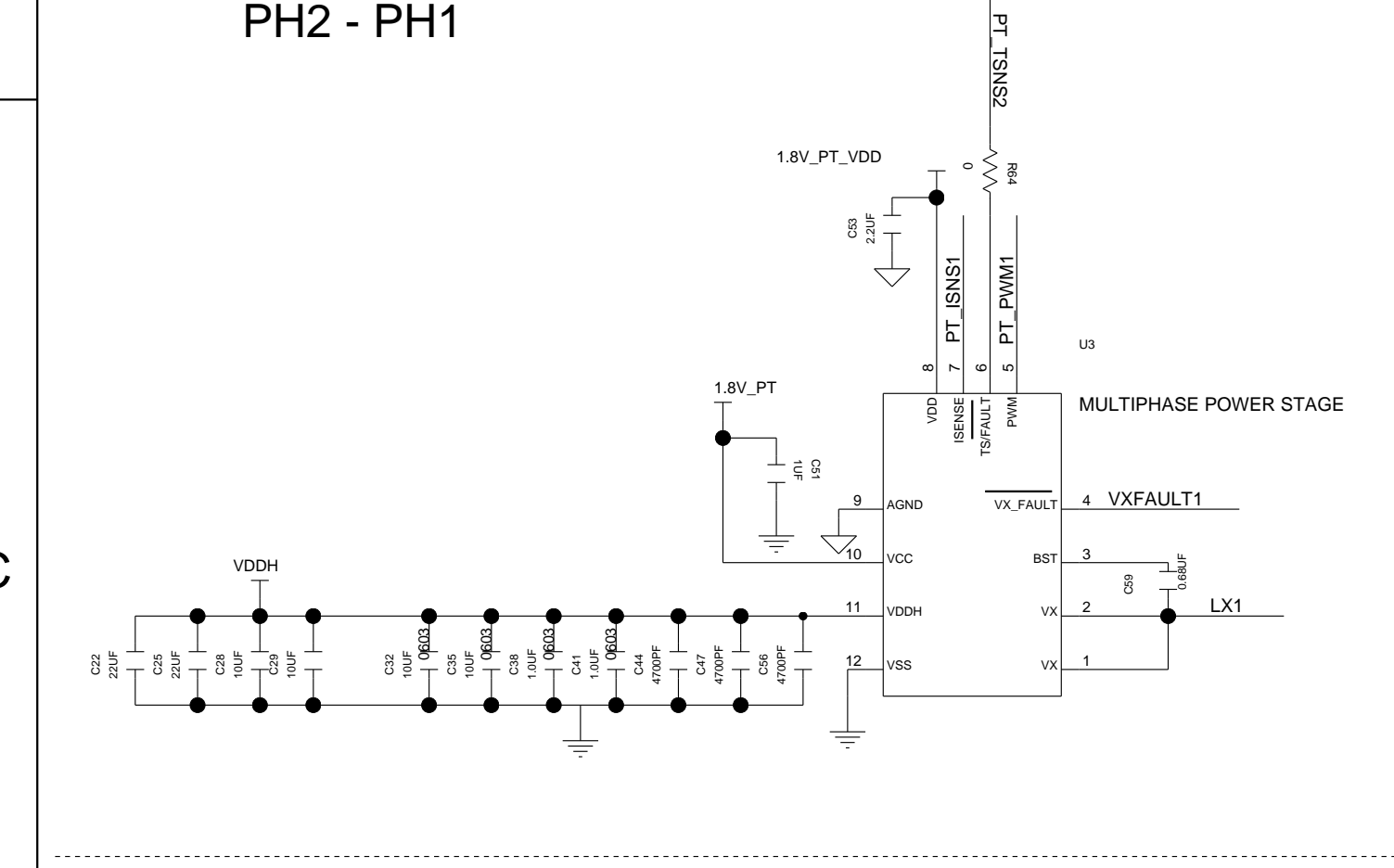
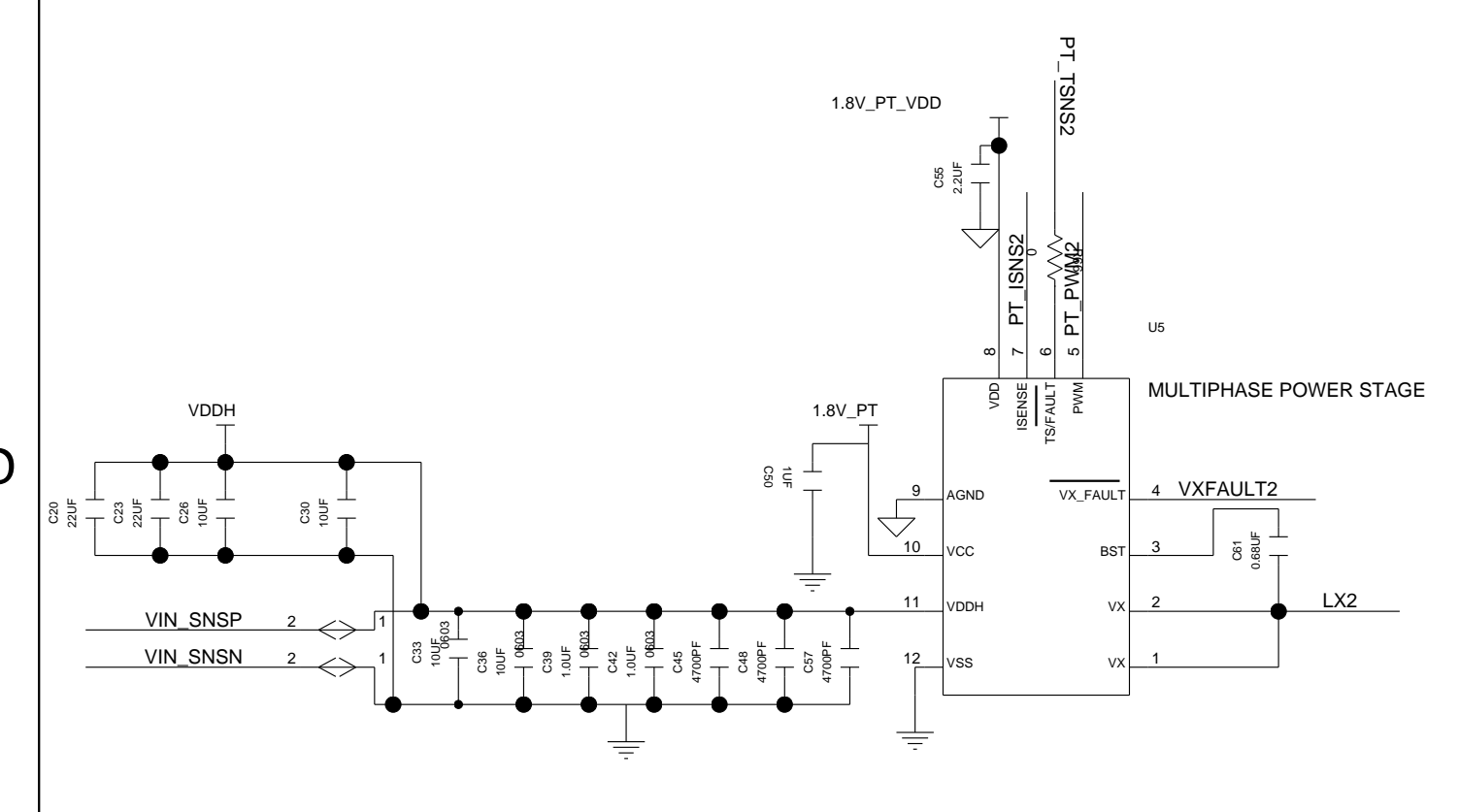
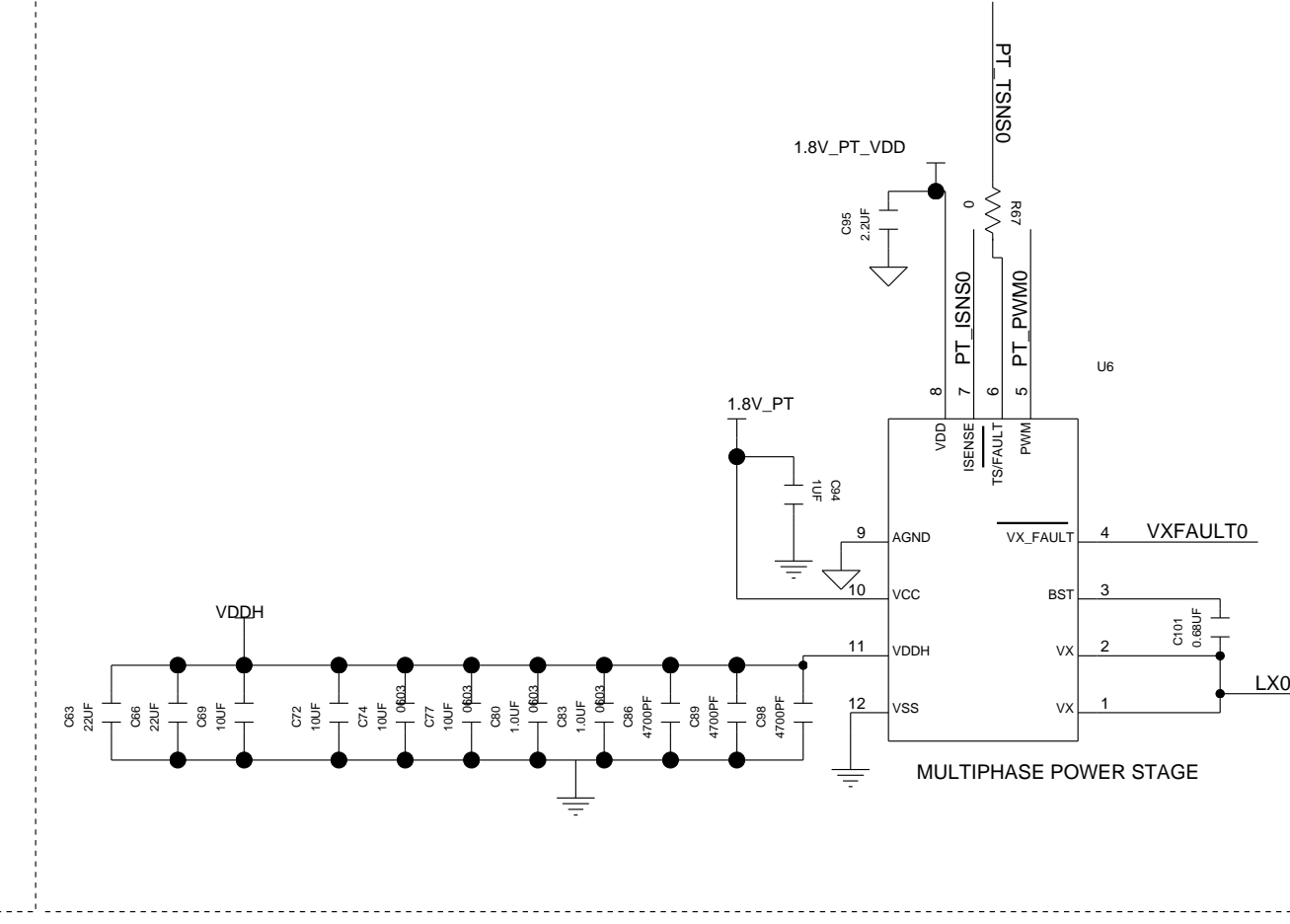
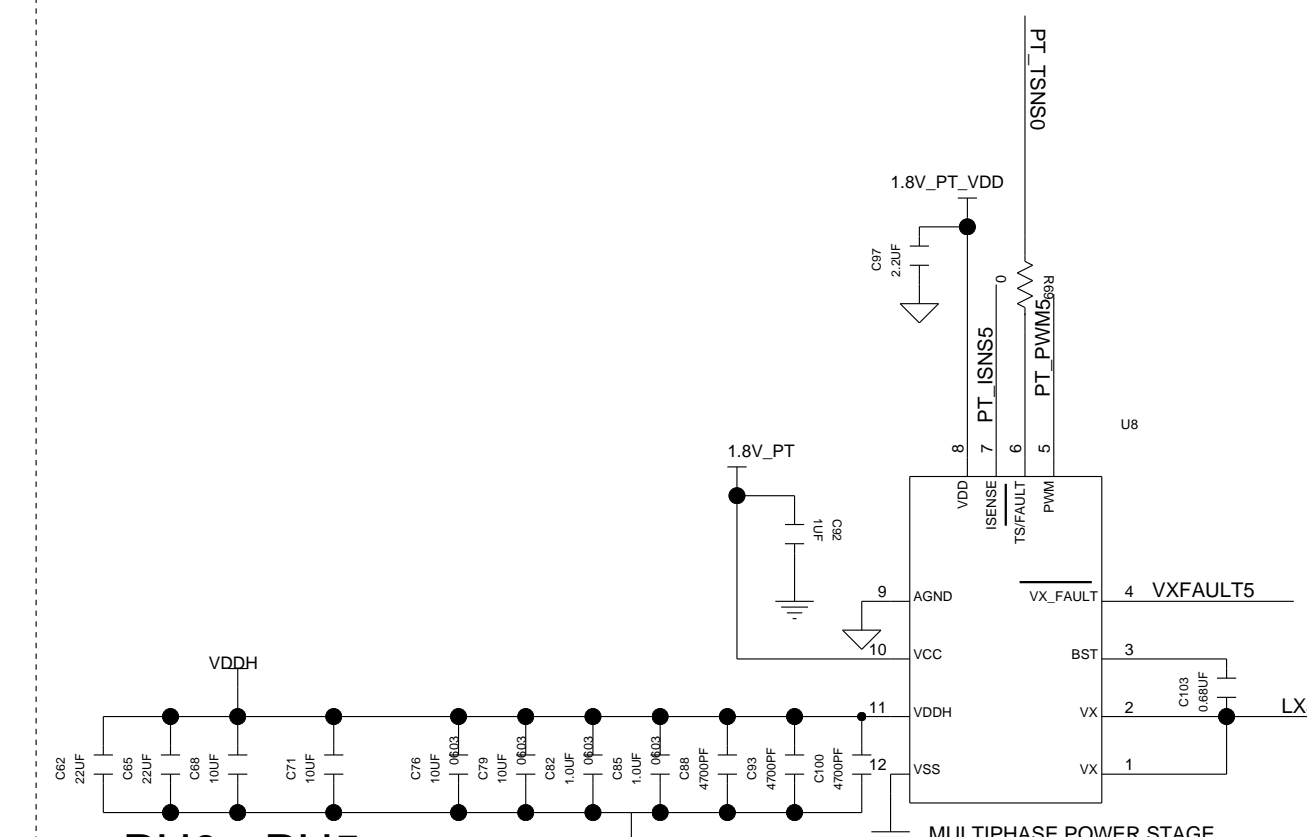
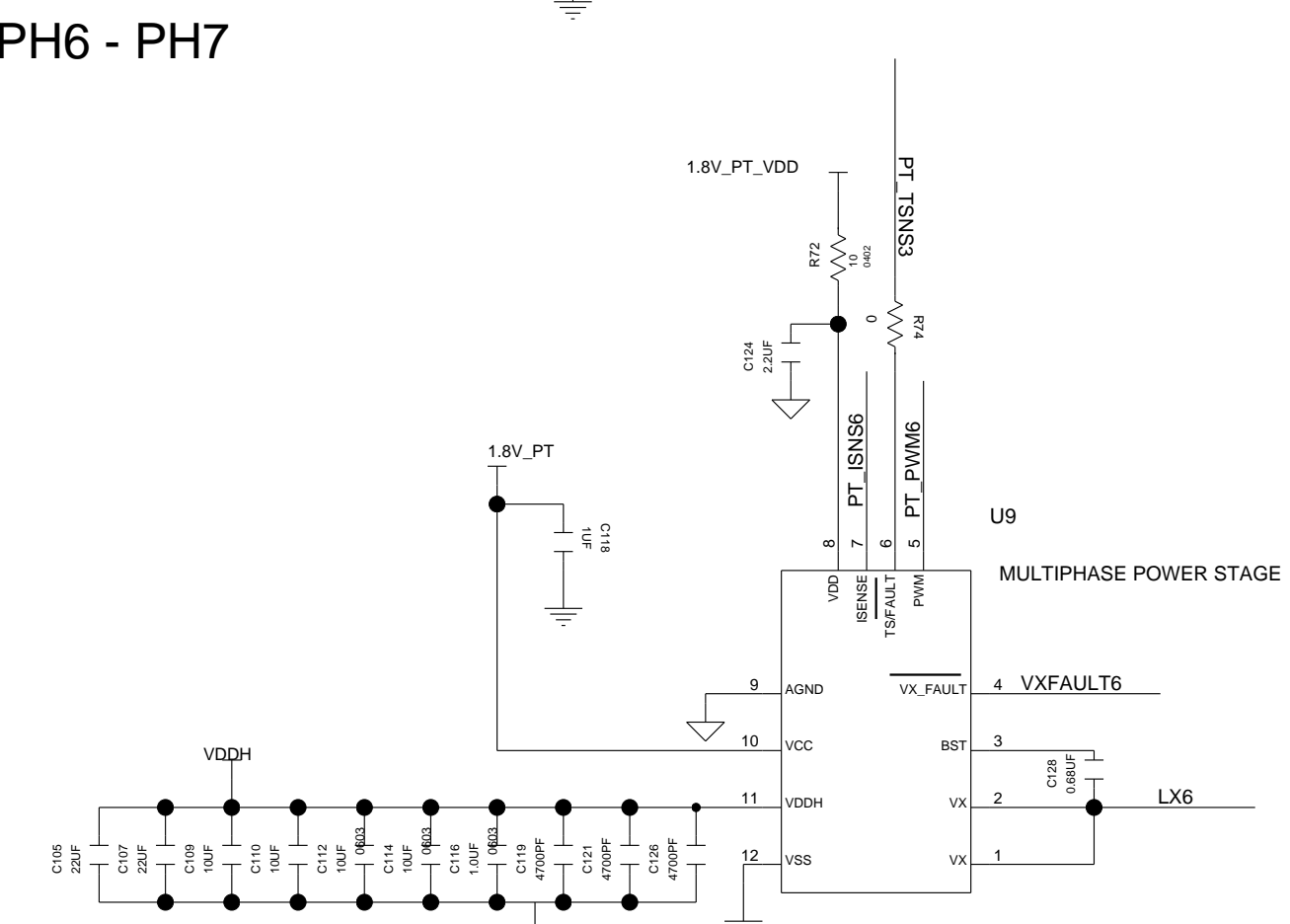
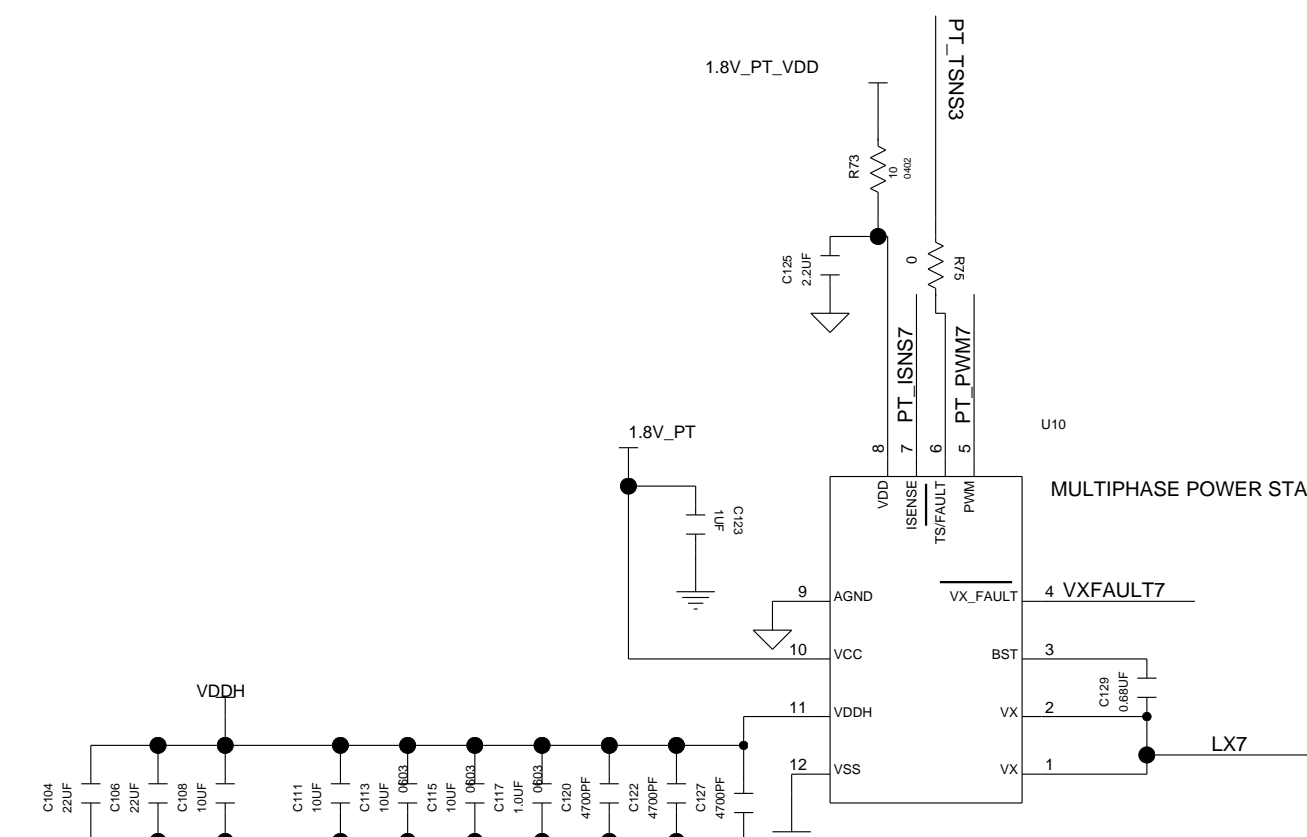
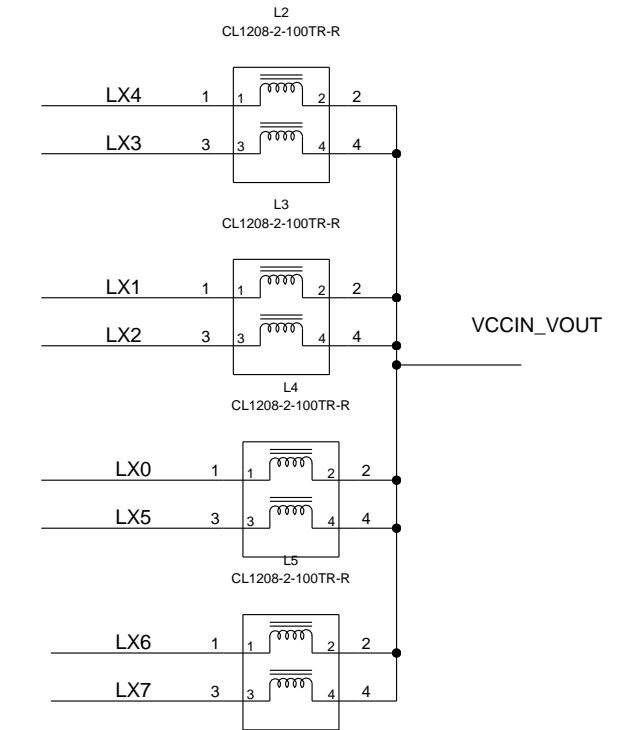


CONNECT TO 1.8V_INT_SW IF THE INTERNAL SWITCHER IS USED

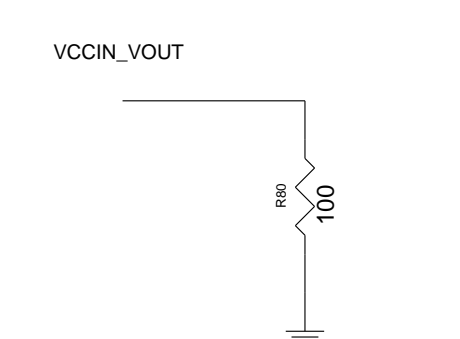


PROJECT TITLE: MAX16602_MAXREFDES1238_APPS_P1		
DRAWING TITLE: PAGE TITLE		
SIZE: D	HARDWARE NUMBER: -	DATE: XXXXXXXX
ENGINEER: -	DRAWN BY: -	REV: P1
TEMPLATE REV: -		SHEET 1 OF 7

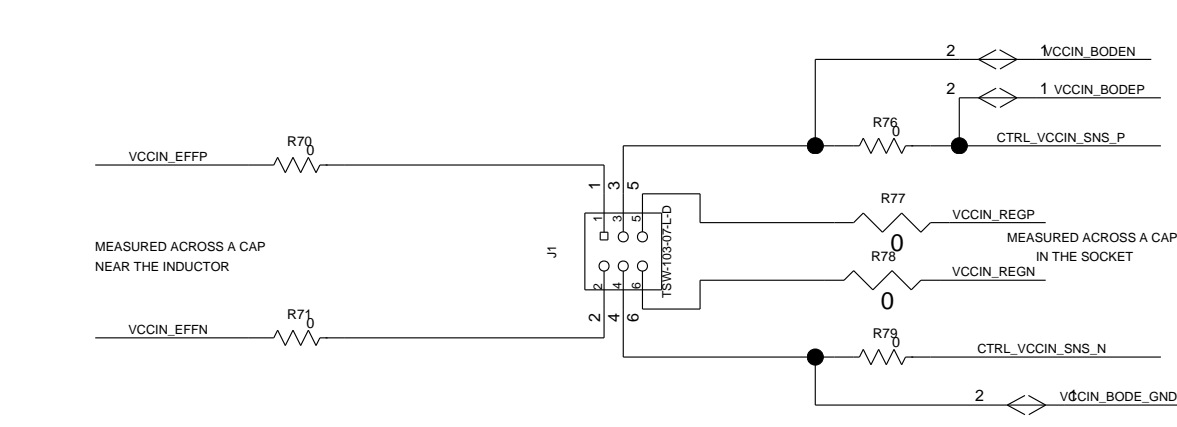
COUPLED INDUCTORS



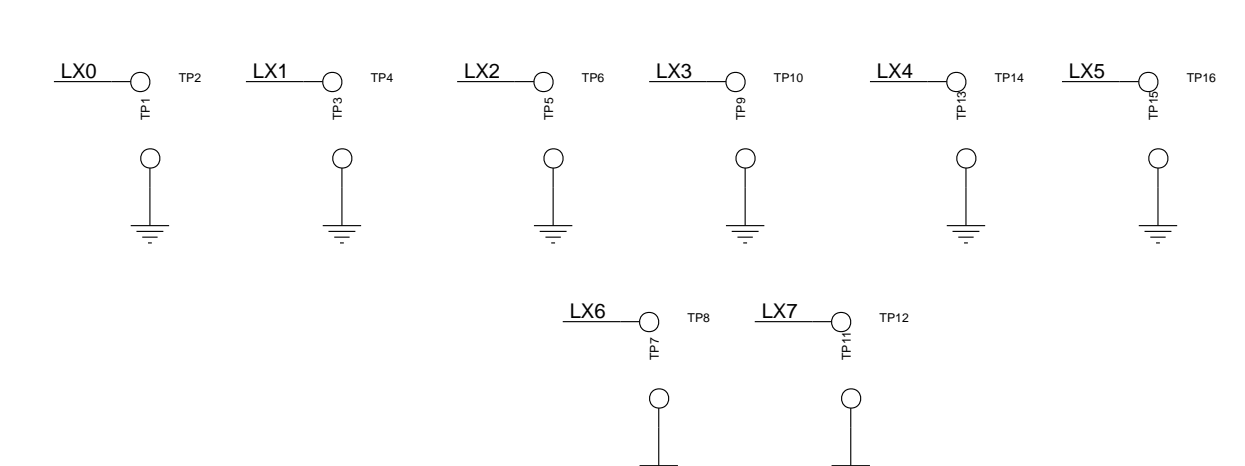
BLEEDER RESISTOR



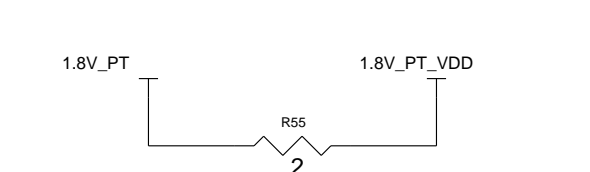
FEEDBACK



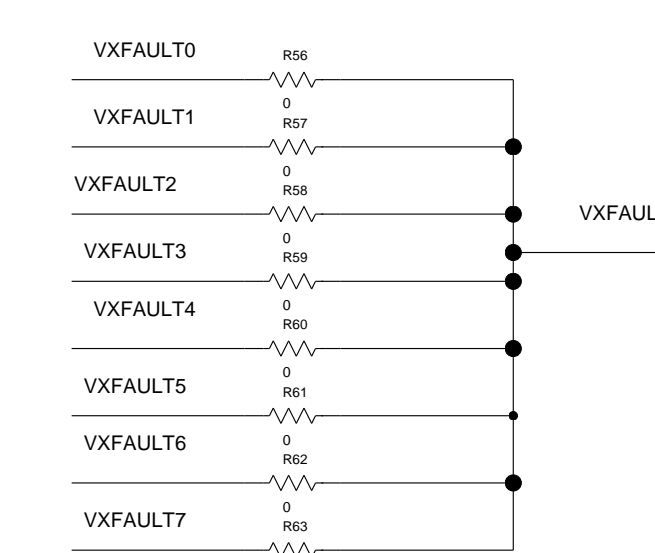
TEST POINT



VDD FILTER RESISTOR



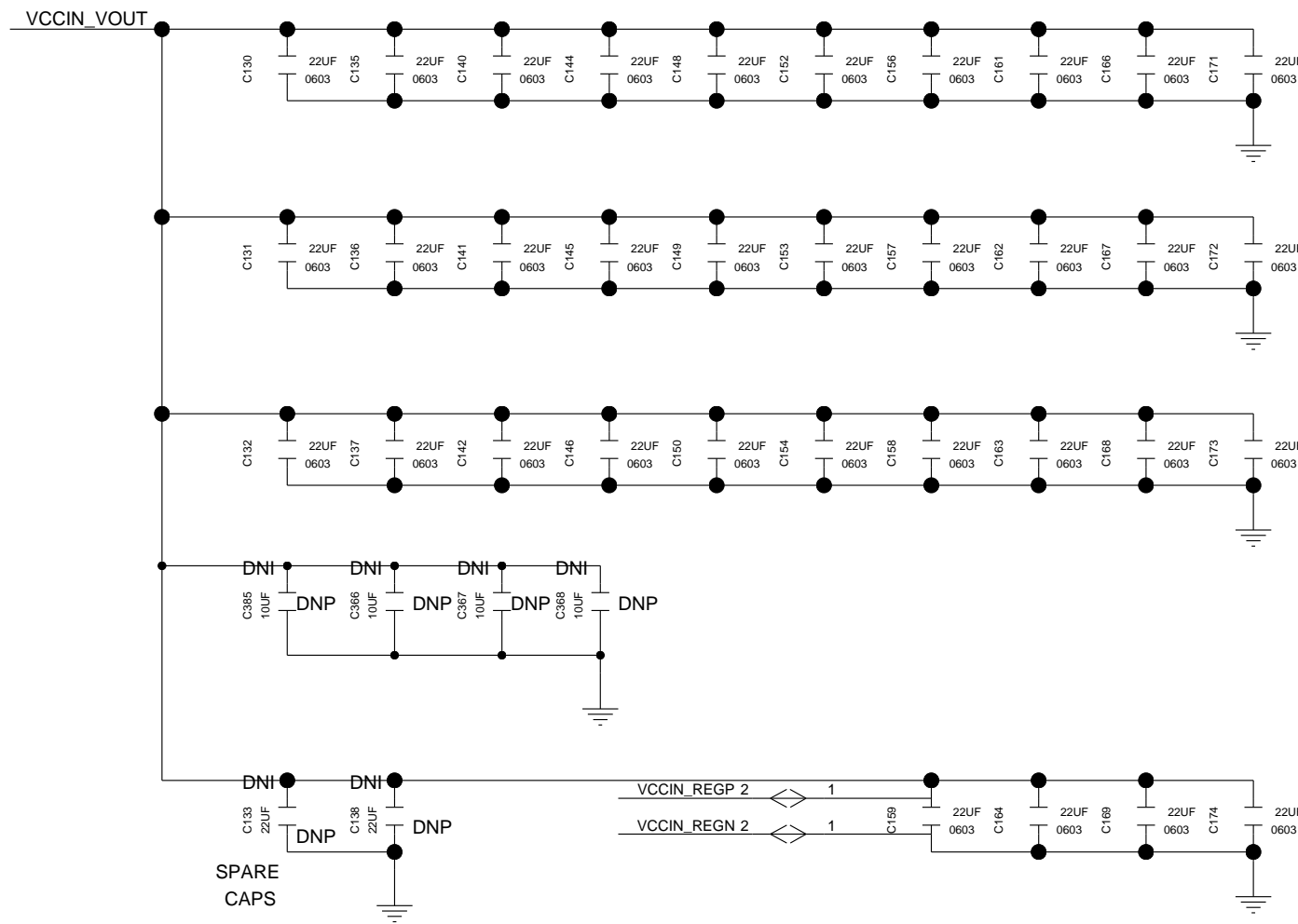
VX FAULT



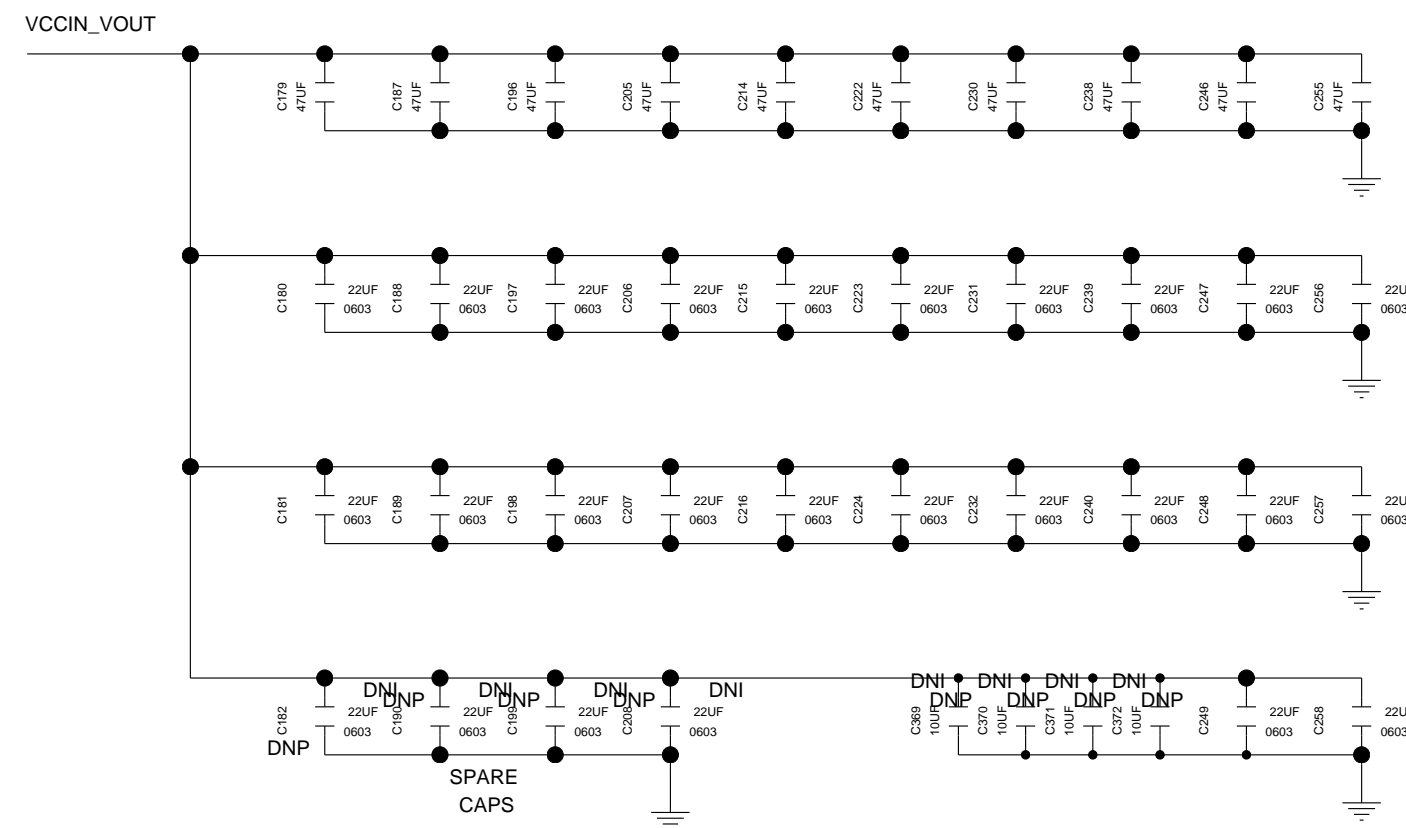
PROJECT TITLE: MAX16602_MAXREFDES1238_APPS_P1		
DRAWING TITLE: PAGE TITLE		
SIZE: D	HARDWARE NUMBER: -	DATE: XXXXXXXX
ENGINEER: -	DRAWN BY: -	REV: P1
TEMPLATE REV: -		SHEET 2 OF 7

VCCIN

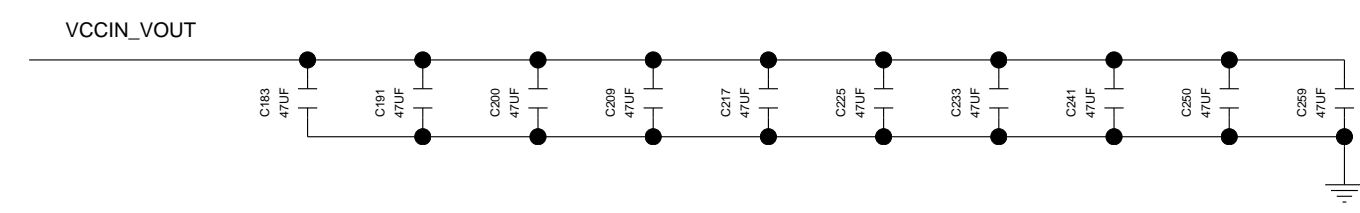
TOP CAVITY 34(+6)X0603



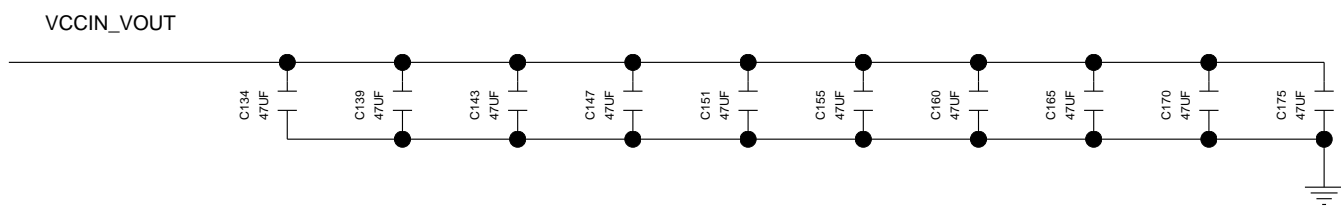
BOT CAVITY 32(+8)X0603



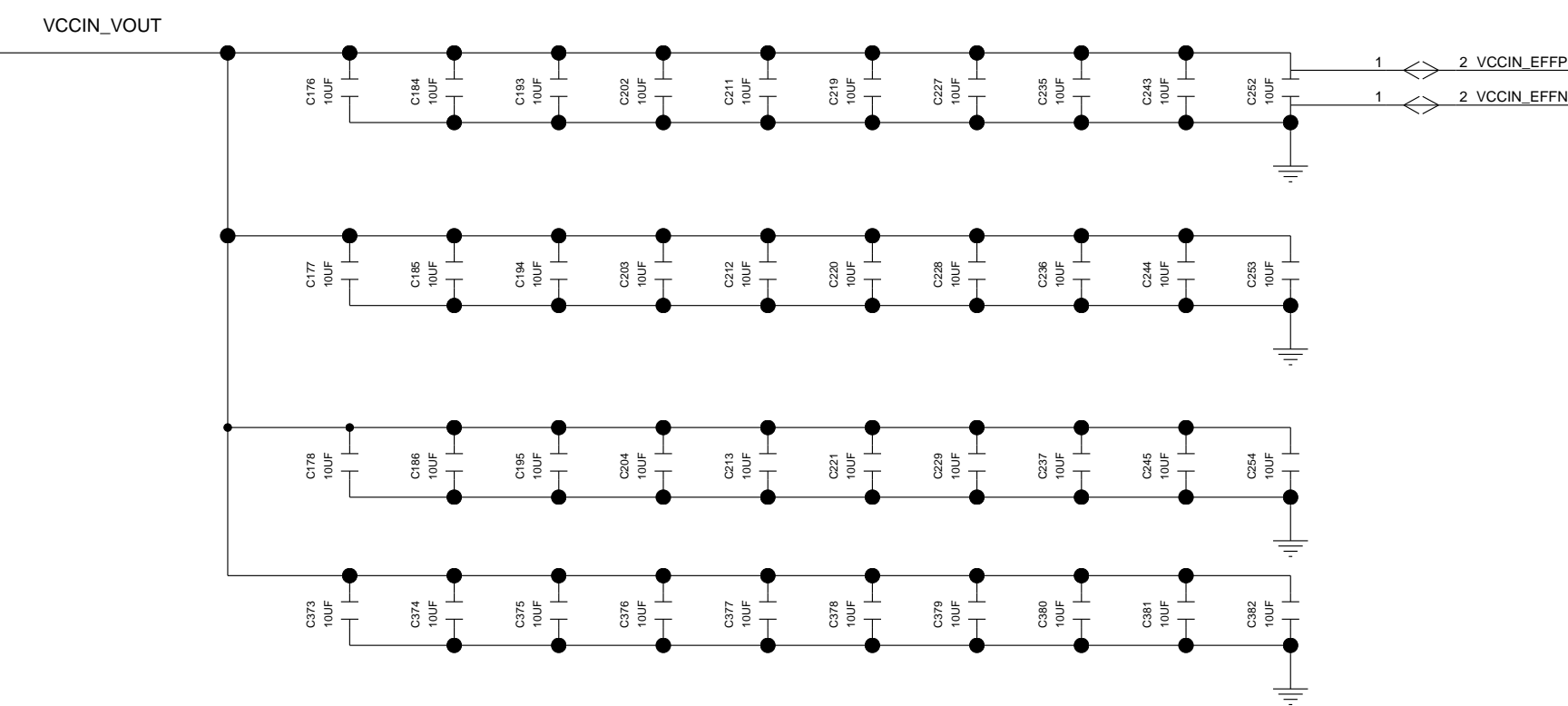
BOT OPENING 10X0805



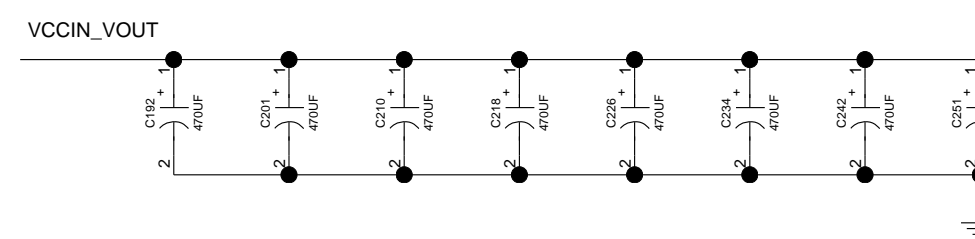
TOP OPENING 10X0805



NEXT TO CL 40X0805

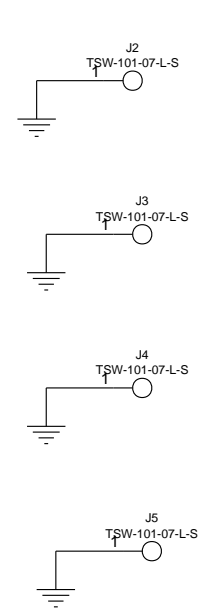


BOT BULK CAPS

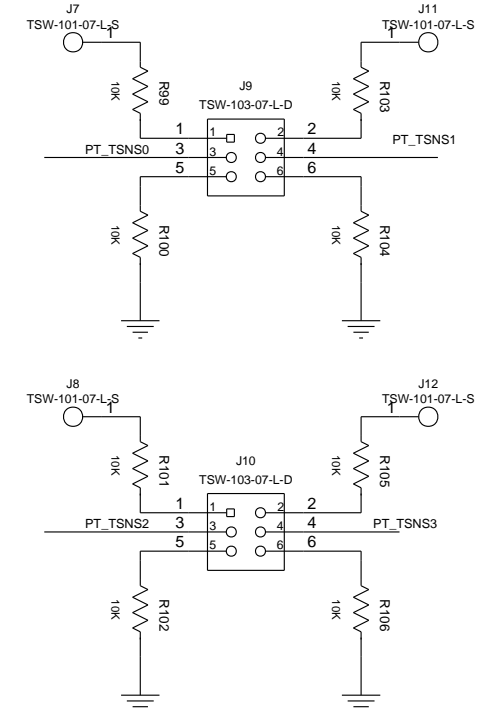


PROJECT TITLE: MAX16602_MAXREFDES1238_APPS_P1		
DRAWING TITLE: PAGE TITLE		
SIZE: D	HARDWARE NUMBER: -	DATE: XXXXXXXX
ENGINEER: -	DRAWN BY: -	REV: P1
TEMPLATE REV: -		SHEET 3 OF 7

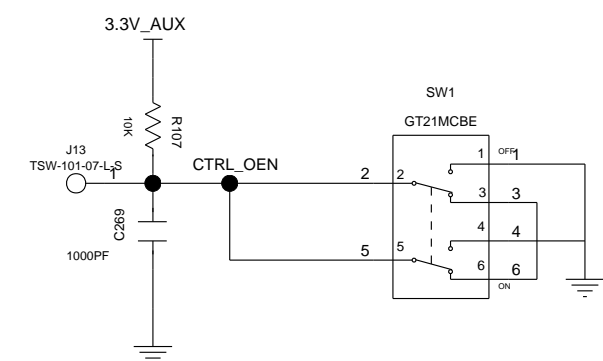
GND PINS



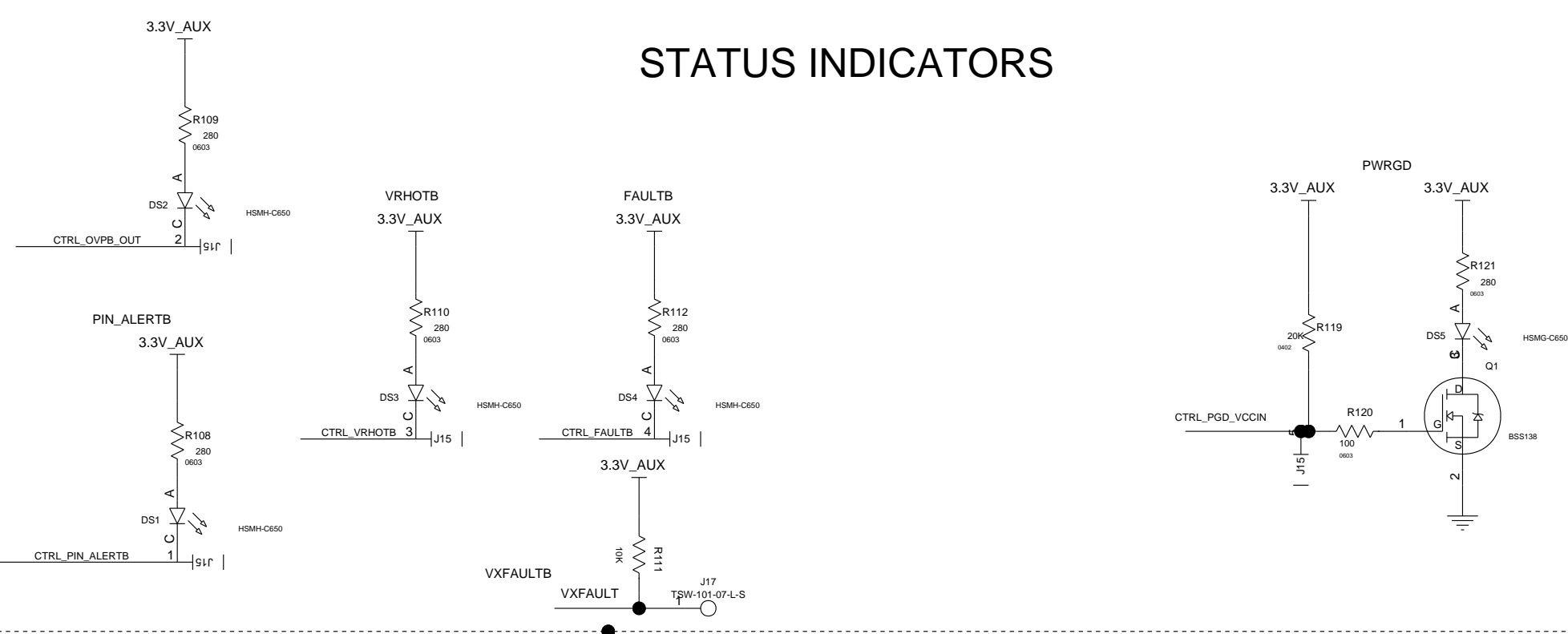
TSNS PULL UP/DOWN



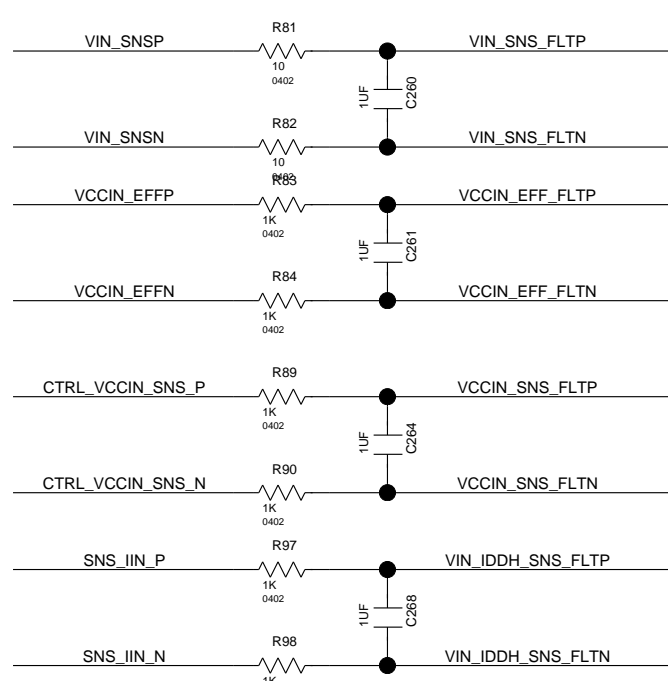
OE SWITCH



STATUS INDICATORS



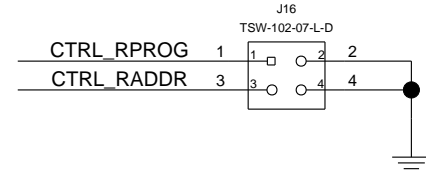
EFFICIENCY



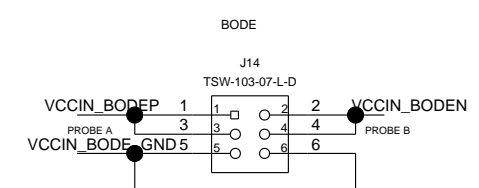
FOR EFFICIENCY

VIN_SNS_FLTP	1	PROG0AAN	2	VIN_SNS_FLTN	VDDH
VCCIN_EFF_FLTP	3	PROG0AAN	4	VCCIN_EFF_FLTN	VOU1_SNS
VCCIN_SNS_FLTP	5	PROG0AAN	6	VCCIN_SNS_FLTN	IDDH
VIN_IDDH_SNS_FLTP	7	PROG0AAN	8	VIN_IDDH_SNS_FLTN	

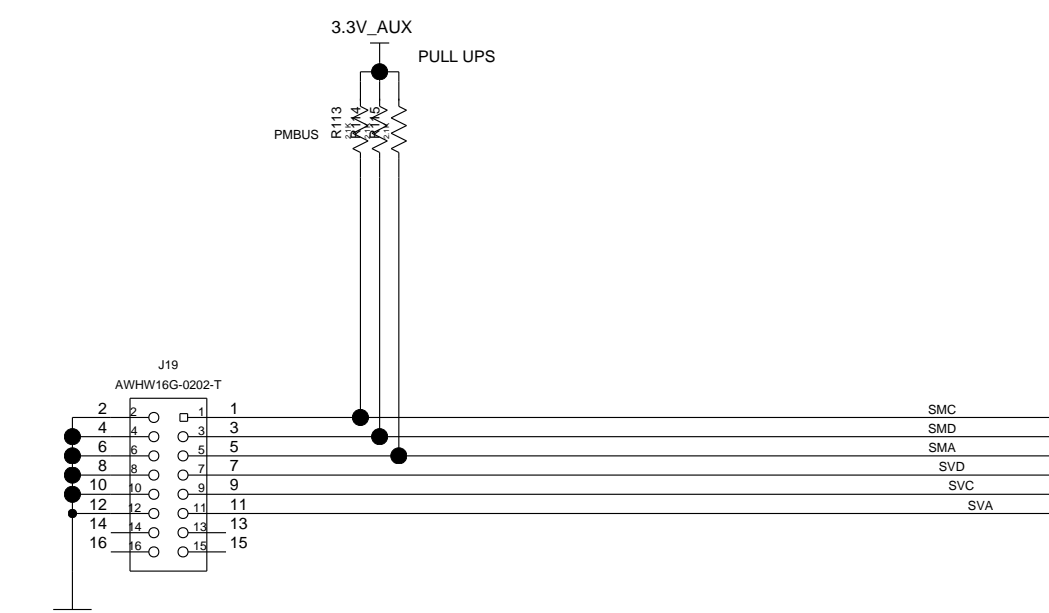
RPROG\RADDR



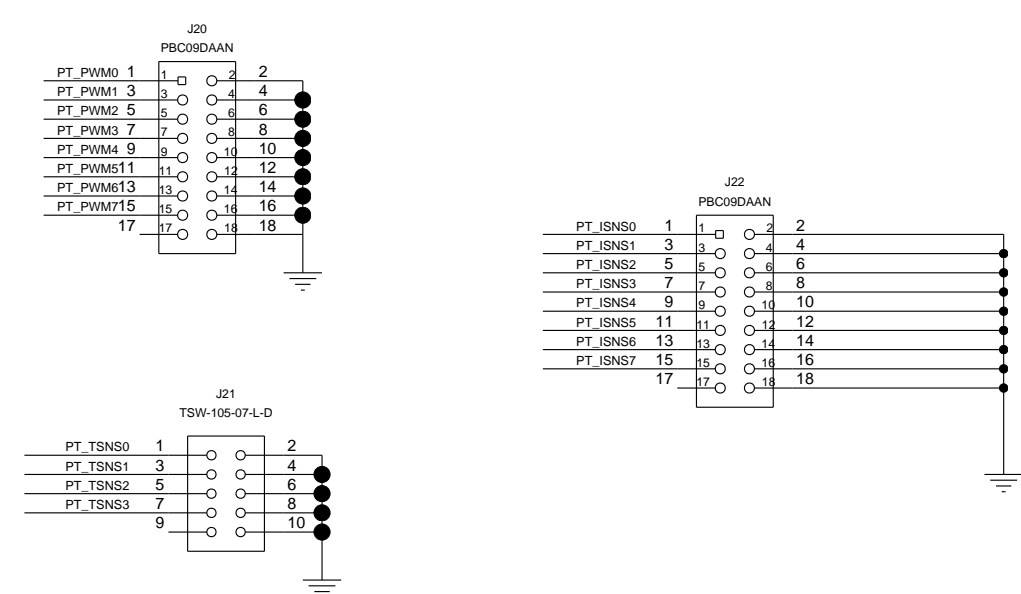
BODE PLOT



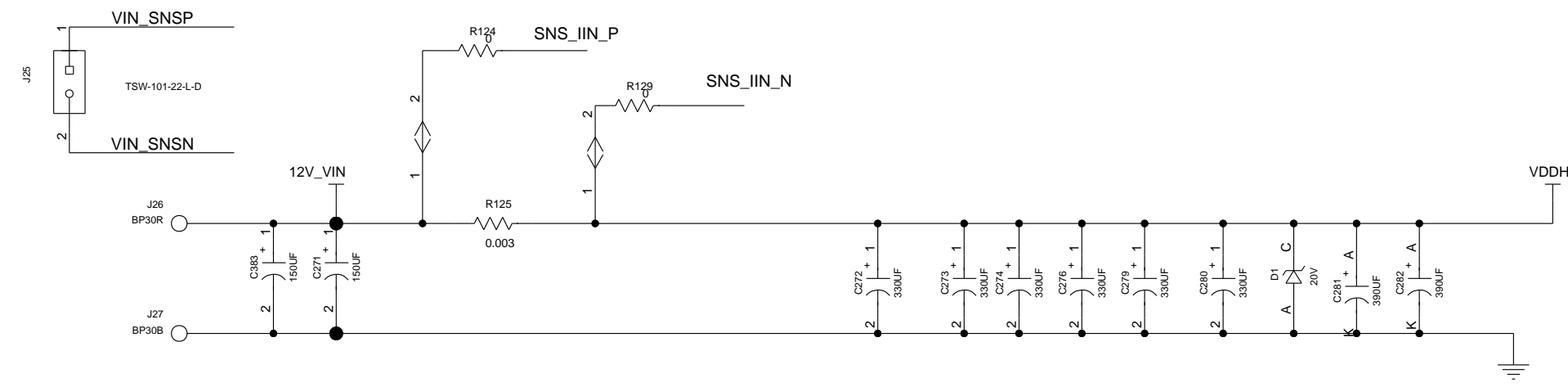
PMBUS\SVID



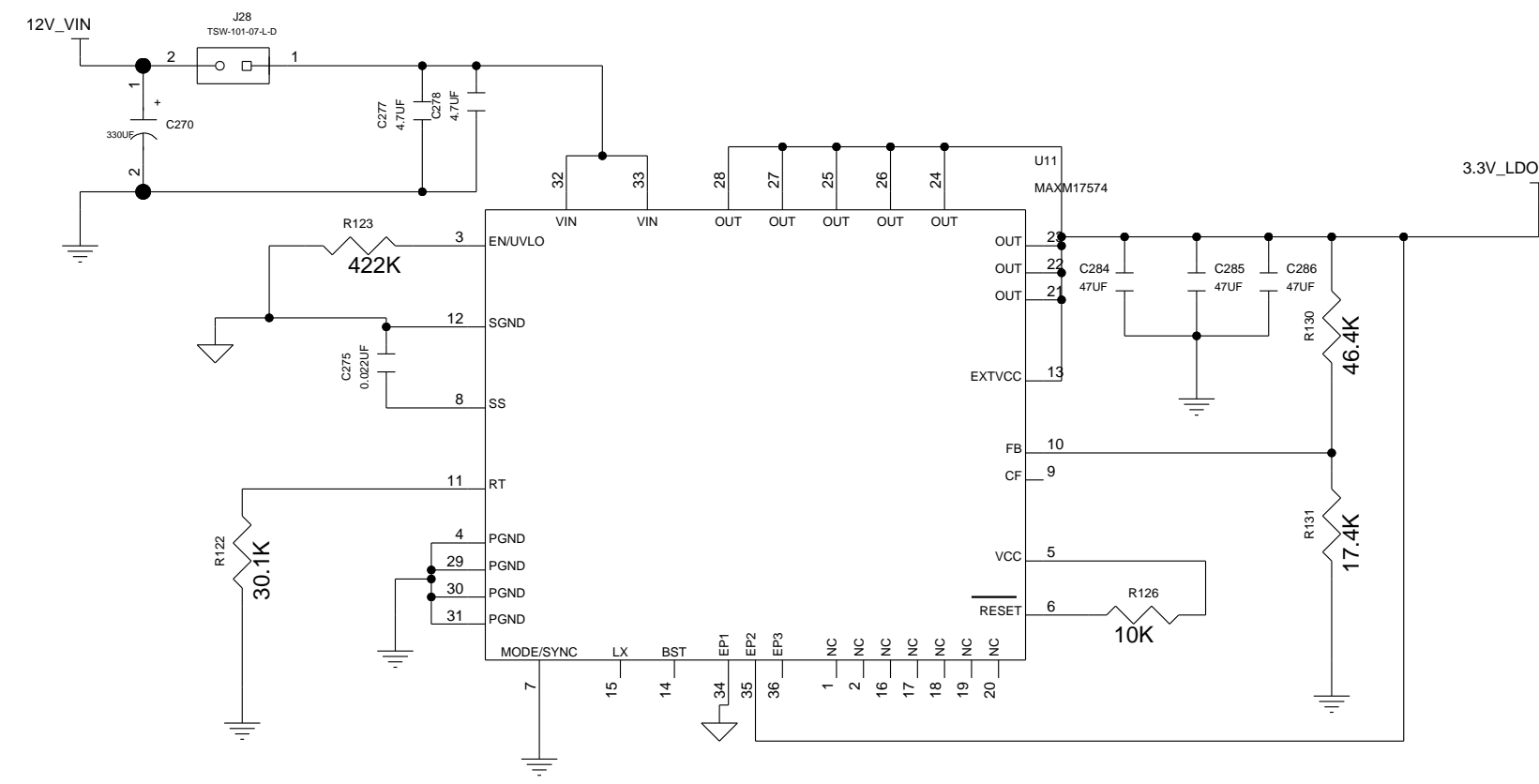
PWM \ ISNS \ TSNS



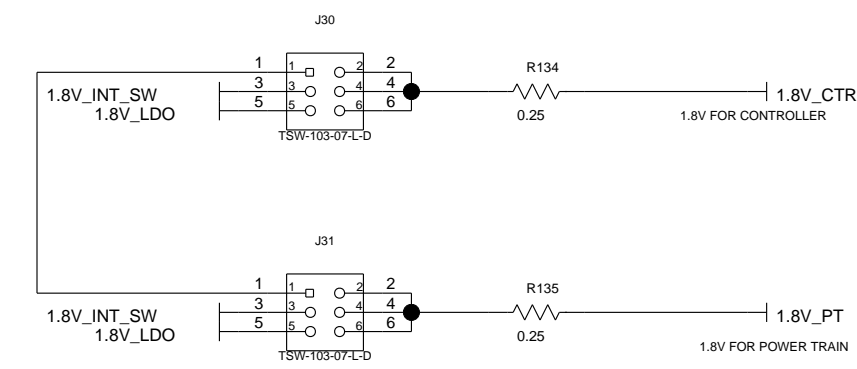
12V INPUT STAGE



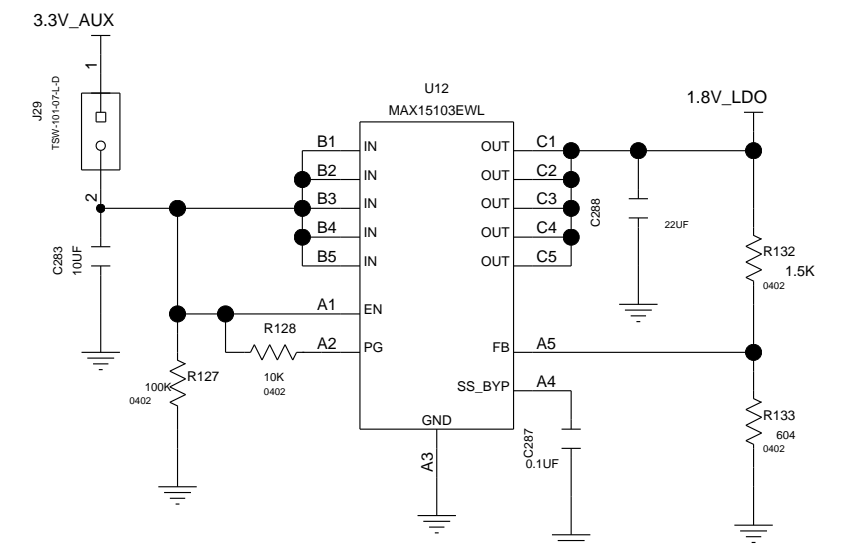
3.3V LDO



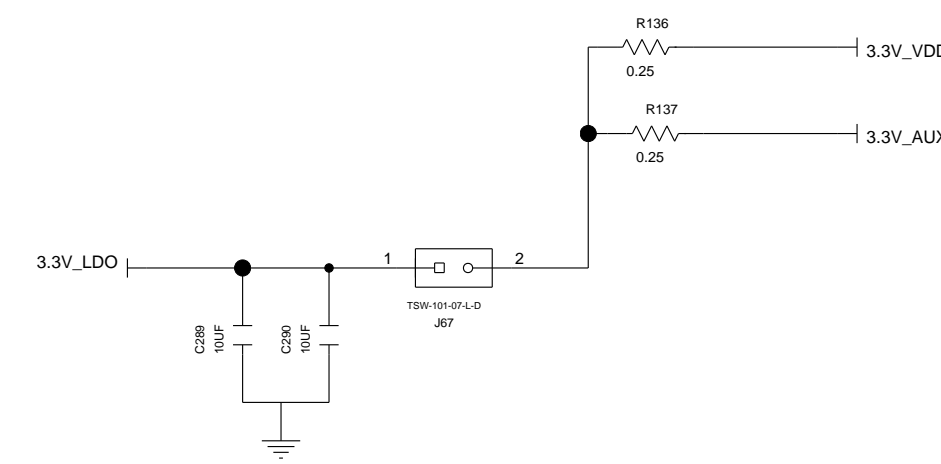
1.8V INPUT STAGE



1.8V LDO

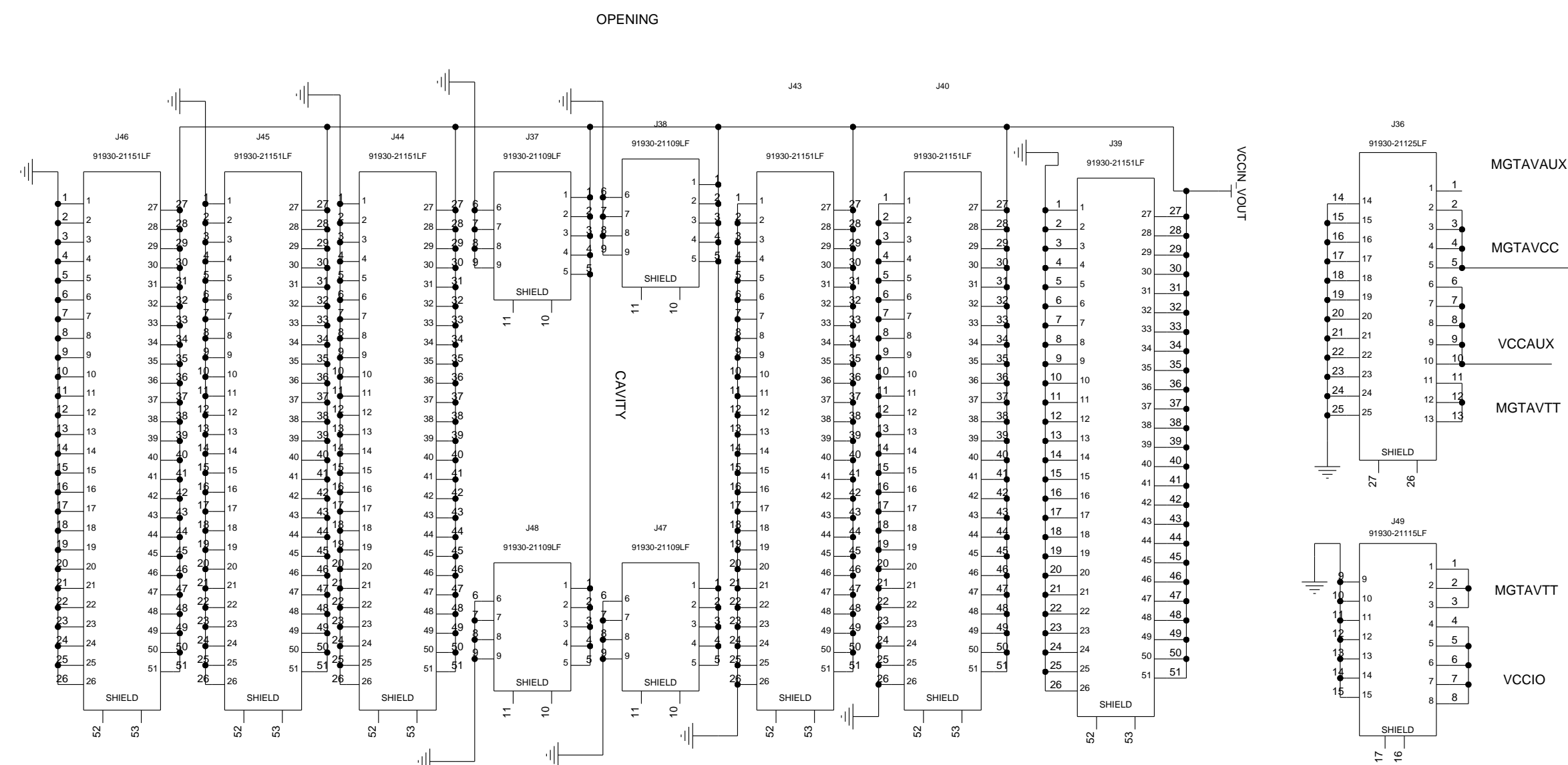


3.3V INPUT STAGE

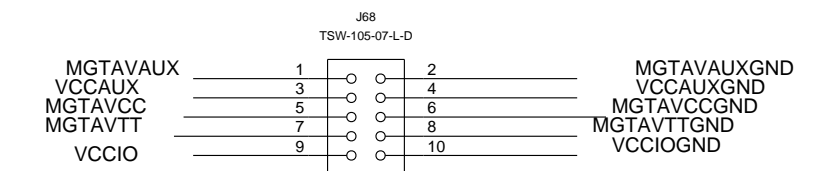
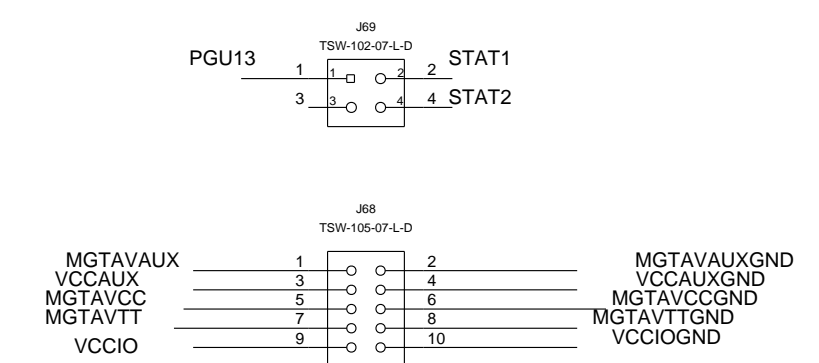
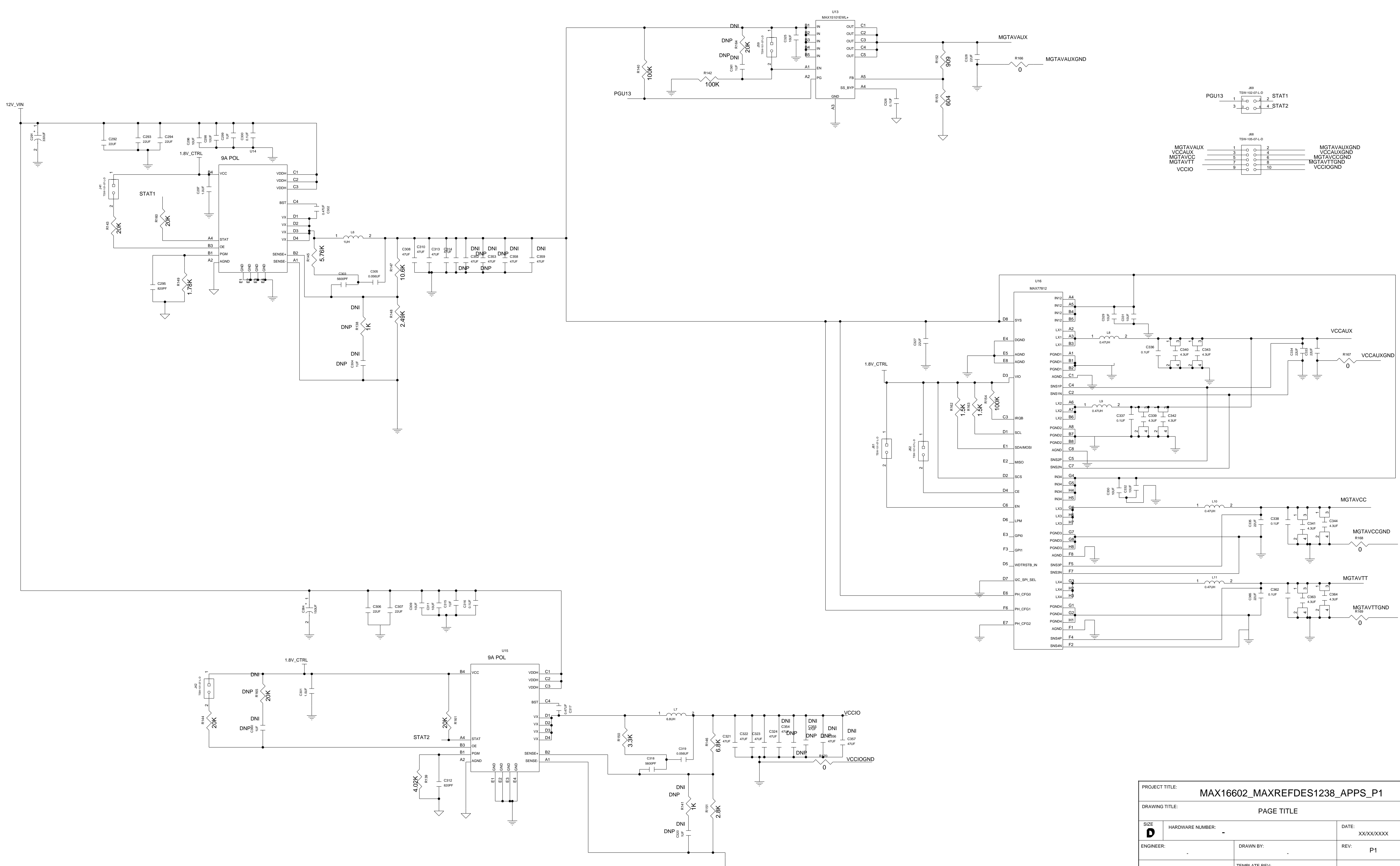


PROJECT TITLE:		MAX16602_MAXREFDES1238_APPS_P1
DRAWING TITLE:		PAGE TITLE
SIZE D	HARDWARE NUMBER:	DATE: XXXXXXXX
ENGINEER:	DRAWN BY:	REV: P1
	TEMPLATE REV:	SHEET 5 OF 7

VERSAL PLATFORM



PROJECT TITLE: MAX16602_MAXREFDES1238_APPS_P1		
DRAWING TITLE: PAGE TITLE		
SIZE: D	HARDWARE NUMBER: -	DATE: XXXXXXXX
ENGINEER: -	DRAWN BY: -	REV: P1
TEMPLATE REV: -		SHEET 6 OF 7



PROJECT TITLE:		MAX16602_MAXREFDES1238_APPS_P1	
DRAWING TITLE:		PAGE TITLE	
SIZE D	HARDWARE NUMBER:	DATE:	XXXXXXXXXX
ENGINEER:	DRAWN BY:	REV:	P1
	TEMPLATE REV:		SHEET 7 OF 7