MAX3963CSA Output Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Component*s.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A0, August 3, 2004

Output Model for the MAX3963

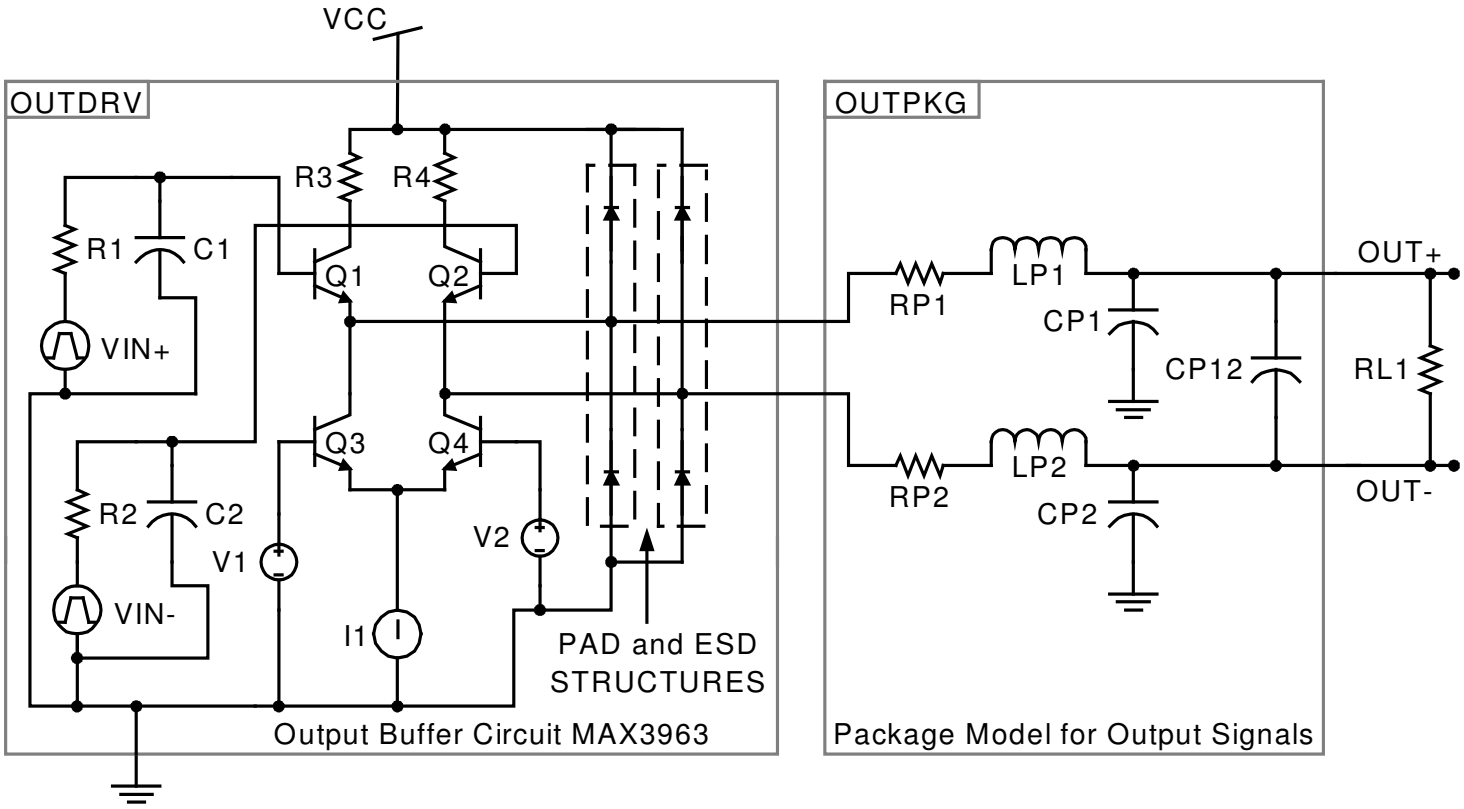

Figure 1. Output model for signal OUT of the MAX3963.

Notes:

The schematics on the previous page represent the output stage of the Maxim MAX3963 155Mbps Transimpedance Preamplifier. The output circuit shown is for the signal outputs (OUT+, OUT-). However the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note, the output signals are described as (2001, 2002). This model is only valid at 25°C. The bias current for the output circuitry is modeled by an ideal current source. This model is compensated for variations in VCC, so VCC equal to 5V should be used.

The Output Stage: The output stage of the MAX3963 is shown as the sub-circuit "OUTDRV".

The OUTDRV Sub-circuit: The outdrv sub-circuit is a simplified version of the output stage used by the MAX3963 Transimpedance Preamplifier. The output stage is terminated differentially with 1kΩ. The output waveform is configured to be at a differential voltage of 1.4V peak to peak. The output common mode voltage has been set to 2.15V. The output waveform has a frequency of 77.5Mhz. The netlist is given in SPICE 2G6 format in Appendix A.

Text File Format: This model is shipped in "pdf" format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the "Text Select Tool." Then the user can "select" what netlist and/or subcircuit with the mouse. Then use the copy command from the "edit" menu to capture the selected lines. These lines can then be "pasted" into the user's text file.

Appendix A: Output Netlist

```
* 3963 Output Model
************************************************
.OPT ACCT NOMOD LIMPTS=10000
.TEMP 25
.OP
.TRAN 2P 30n
************************************************

* Voltage Source
VCC 101 0 5
* Load Resistance
RL1 2001 2002 1k

************************************************
XOUTPKG 2001 2002 50 51 OUTPKG
XOUTDRV 50 51 101 OUTDRV
************************************************

************************************************
.SUBCKT OUTDRV 50 51 101

VINP 1  0 PULSE (2.62 3.341 0.04n 0.40n 0.40n 6.0n 12.9032n)
VINN 3  0 PULSE (3.341 2.62 0.04n 0.40n 0.40n 6.0n 12.9032n)
V1 6 0 1V
V2 7 0 1V

R1 2 1 50
R2 4 3 50
R3 101 8 100
R4 101 9 100

C1 2 0 12p
C2 4 0 12p

XQ1 8 2 50 0 H11A05_4
XQ2 9 4 51 0 H11A05_4
XQ3 50 6 5 0 H11A05_3
XQ4 51 7 5 0 H11A05_3

I1 5 0 5mA

CP1 50 0 .1p
CP2 51 0 .1p
```

```
.ENDS OUTDRV
************************************************

************************************************
.SUBCKT OUTPKG 2001 2002 50 51

RP1    50  500 340M
RP2    51  501 340M
LP1   500 2001 .83N
LP2   501 2002 .83N
CP1  2001    0 178F
CP2  2002    0 178F
CP12 2001 2002 1F

.ENDS OUTPKG
************************************************

************************************************
.SUBCKT H11A05_4 1 2 3 21
CP1EPI 1 2 15.796F
CP1P2 12 3 25.890F
CTRENCH 1 20 34.441F
RBX 2 12 15.269 TC=2.649M
RCX 1 10 10.075 TC=2.883M,1.658U
RCI 10 11 530.265M TC=2.883M,1.658U
REX 13 3 2.164 TC=182.441U
RSUB 20 21 2.962K
QP 20 10 12 20 TXP 4 OFF
QN 11 12 13 11 TX 4
.MODEL TX NPN( IS=1.151E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=44.016M
+   IKR=806.400U ISE=5.444E-021 ISC=7.000E-030 RB=61.077 RBM=45.808
+   IRB=7M CJE=37.151F MJE=490M VJE=940M FC=990M CJC=7.359F MJC=470M
+   VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=20.430M PTF=5 KF=1.500F
+   AF=1 )
.MODEL TXP PNP( IS=6.540E-019 CJE=7.359F MJE=470M VJE=850M CJC=9.940F
+   MJC=400M VJC=650M BF=10K BR=672.167U TF=1N FC=900M )
.ENDS H11A05_4
************************************************

************************************************
.SUBCKT H11A05_3 1 2 3 21
CP1EPI 1 2 11.847F
CP1P2 12 3 19.418F
CTRENCH 1 20 25.831F
RBX 2 12 20.359 TC=2.649M
```

```
RCX 1 10 13.433 TC=2.883M,1.658U
RCI 10 11 707.020M TC=2.883M,1.658U
REX 13 3 2.885 TC=182.441U
RSUB 20 21 3.949K
QP 20 10 12 20 TXP 3 OFF
QN 11 12 13 11 TX 3
.MODEL TX NPN( IS=1.151E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=44.016M
+   IKR=806.400U ISE=5.444E-021 ISC=7.000E-030 RB=61.077 RBM=45.808
+   IRB=7M CJE=37.151F MJE=490M VJE=940M FC=990M CJC=7.359F MJC=470M
+   VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=20.430M PTF=5 KF=1.500F
+   AF=1 )
.MODEL TXP PNP( IS=6.540E-019 CJE=7.359F MJE=470M VJE=850M CJC=9.940F
+   MJC=400M VJC=650M BF=10K BR=672.167U TF=1N FC=900M )
.ENDS H11A05_3
**********************************************

.PROBE
.END
```