MAX3822 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Component*s.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

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I/O Models for the MAX3822

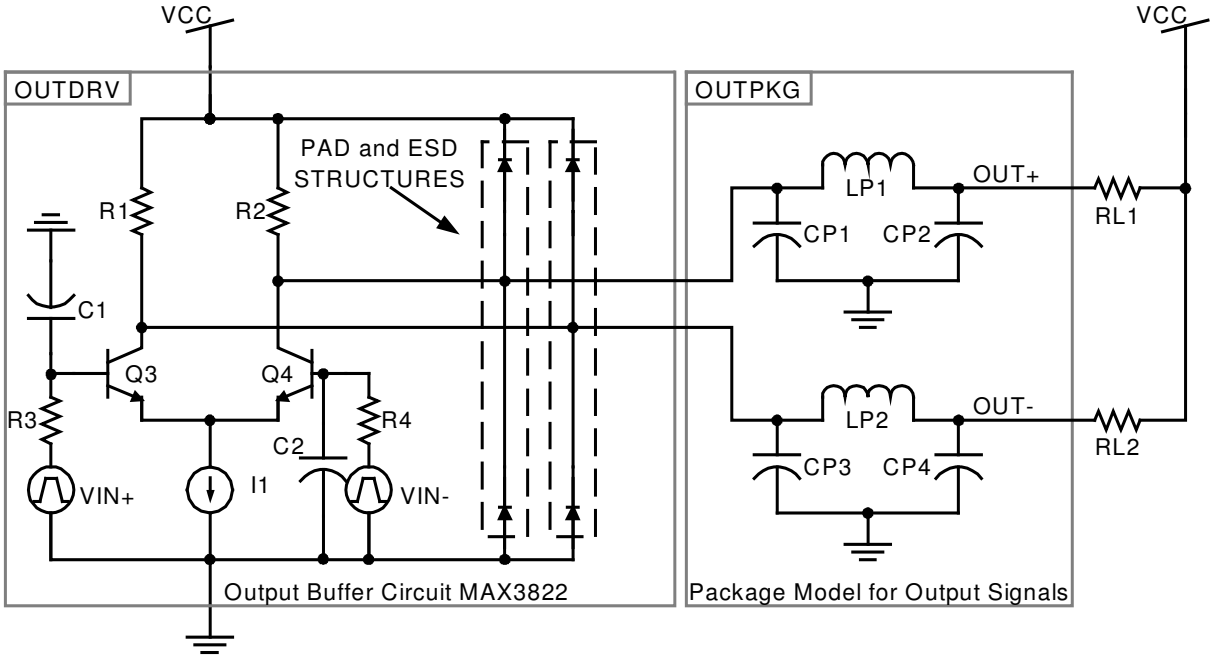

Figure 1. Outbut signal buffer for the MAX3822.

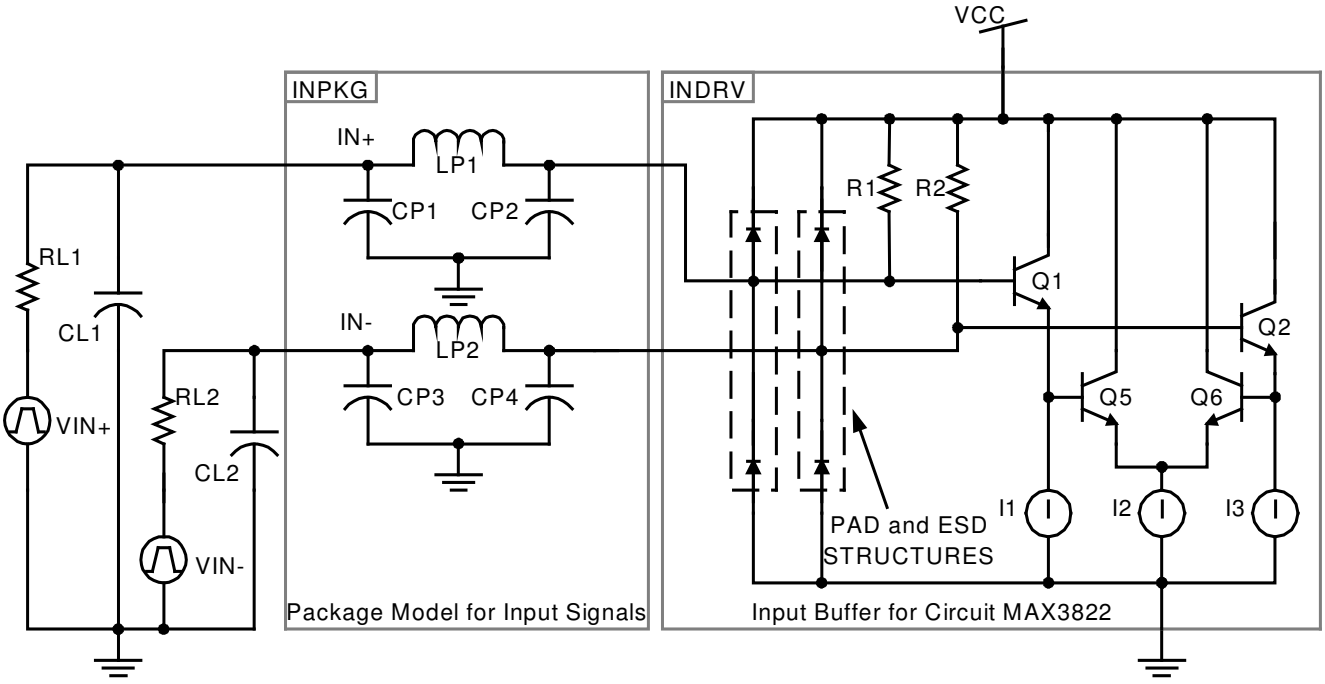

Figure 2. Input signal buffer for the MAX3822

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3822 2.5Gbps Quad Limiting Amplifier. The output circuit shown is for the signal outputs (OUT+, OUT-) and the input circuit is shown with the signal inputs (IN+, IN-). However the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note the output signals are described as (2001, 2002) and the input signals are described as (2101, 2102). These models are only valid at 25°C. The bias currents for the input and output circuitry are modeled by ideal current sources. This model is not compensated for variations in VCC, so VCC equal to 3.3V should be used. The package used for both stages consists of a 1.5nH inductor that has a .4pF and .2pF capacitor on either side of the inductor. The pad structure is included with the package.

The Output Stage: The output stage of the MAX3822 is shown as the sub-circuits "OUTDRV" and "OUTPKG".

The DRV Driver Sub-circuit: The driver sub-circuit is a simplified version of the output stage used by the MAX3822 Quad Limiting Amplifier. The output load is configured with 50 ohm resistors tied to VCC. Adjusting I1 causes the output levels to change. I1 equal to 14.73mA has an output of 740mV peak to peak, while I1 equal to 12.41mA and 20mA leads to outputs of 640mV peak to peak and 1000mV peak to peak respectively. The output is currently configured to be at 740mV peak to peak with rise and fall times of approximately 90ps and a common mode output voltage of 3.1V. This model is designed to work at an output differential of 740mV. Changing this level is not supported as other parameters are also affected. The signal sources in the output stage are modeled by ideal voltage generators whose signal swings are from 1.5 to 2 Volts. The output driver is a differential pair (Q1, Q2) is implemented with four H14E04 transistors in parallel for both Q1 and Q2. In Appendix A the netlist is given in SPICE 2G6 format.

The Input Stage: The input structure of the MAX3822 connects to a common emitter configuration. The input stage has sub-circuits "INDRV" and "INPKG".

The DRV Driver Sub-circuit: The input structure of the MAX3822 is connected to an equivalent resistive, capacitive and inductive network of the input package. The input package connects to a common emitter configuration. The driving voltage source should be set to 0V differential at t=0. This ensures that the two AC coupling capacitors are not charged to different voltages initially (this is the way the circuit operates in steady-state operation). This was achieved by using a piecewise linear source as the driver. See Appendix B for the input netlist.

Text File Format: This model is shipped in "pdf" format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the "Text Select Tool." Then the user can "select" what netlist and/or subcircuit with the mouse. Then use the copy command from the "edit" menu to capture the selected lines. These lines can then be "pasted" into the user's text file.

Appendix A: Output Netlist

```
* 3822 Output Model
**********************************************
.OPT ACCT NOMOD LIMPTS=10000
.TEMP 25
.OP
.TRAN 2P 4n
**********************************************

* Voltage Source
VCC 101 0 3.3
* Load Resistances
RL1 2001 101 50
RL2 2002 101 50

**********************************************
XOUTPKG 2001 2002 50 51 OUTPKG
XOUTDRV 50 51 101 OUTDRV
**********************************************

**********************************************
.SUBCKT OUTDRV 50 51 101

* Driving Voltage
VINP 20 0 PULSE (1.5 2 0.04n 30p 30p 430p 888.5p)
VINN 21 0 PULSE (2 1.5 0.04n 30p 30p 430p 888.5p)
R3 20 1 50
R4 21 3 50
C1 1 0 6.2p
C2 3 0 6.2p

* Differential Pair
XQ3 50 1 5 0 H14E04_4
XQ4 51 3 5 0 H14E04_4

* Change I1 to change the output differential voltage.
I1 5 0 14.73mA

R1 101 50 50
R2 101 51 50

* ESD Structure
XD1  50 101 0 HDE113032
XD2   0  50 0 HDE113032
XD3  51 101 0 HDE113032
```

```
XD4   0  51 0 HDE113032

.ENDS OUTDRV
************************************************

************************************************
.SUBCKT OUTPKG 2001 2002 50 51

LP1   50 2001 1.5N
LP2   51 2002 1.5N
CP1   50    0 .4pF
CP2   51    0 .2pF
CP3 2001    0 .4pF
CP4 2002    0 .2pF

.ENDS OUTPKG
************************************************

************************************************
* Q1 and Q2 Transistor Model
.SUBCKT H14E04_4 1 2 3 21
CP1EPI 1 2 48.738F
CP1P2 12 3 78.537F
CTRENCH 1 20 61.228F
RBX 2 12 5.139 TC=2.663M
RCX 1 10 5.877 TC=2.354M,979.573N
RCI 10 11 309.325M TC=2.354M,979.573N
REX 13 3 698.690M TC=123.150U
RSUB 20 21 1.549K
QP 20 10 12 20 TXP 4 OFF
QN 11 12 13 11 TX 4
.MODEL TX NPN( IS=3.326E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=126.546M
+   IKR=2.318M ISE=1.573E-020 ISC=2.022E-029 RB=20.554 RBM=15.416
+   IRB=20.223M CJE=107.672F MJE=490M VJE=940M FC=990M CJC=21.929F
+   MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=59.621M PTF=5
+   KF=1.500F AF=1 )
.MODEL TXP PNP( IS=1.968E-018 CJE=21.929F MJE=470M VJE=850M CJC=21.582F
+   MJC=400M VJC=650M BF=10K BR=809.067U TF=1N FC=900M )
.ENDS H14E04_4
************************************************

************************************************
* ESD Diode Model
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
```

```
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+   VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
**********************************************

.PROBE
.END
```

Appendix B: Input Netlist

```
* 3822 Input Model
**********************************************
.OPT ACCT NOMOD LIMPTS=10000
.TEMP 25
.OP
.TRAN 2P 2n
**********************************************

* Voltage Source
VCC 101 0 3.3V

**********************************************
*  Add input source here.
*  The source should connect to node 50 (VINP)
*  and 60 (VINN).
*  Example:
VINP  50 0 PULSE (.8 .5 .2n .01n .01n .3n .62n)
VINN  60 0 PULSE (.5 .8 .2n .01n .01n .3n .62n)

RL1 2101 50 50
RL2 2102 60 50
CL1 2101  0 1.8p
CL2 2102  0 1.8p
**********************************************

**********************************************
XINPKG 2101 2102 2000 2001 INPKG
XINDRV 2000 2001 101 INDRV
**********************************************

**********************************************
.SUBCKT INDRV 2000 2001 101

R1 2000 101 50
R2 2001 101 50

XQ1 101 2001 5 0 H11A05
XQ2 101 2000 6 0 H11A05
XQ5 101    6 7 0 H11A05
XQ6 101    5 7 0 H11A05

I1 6 0 10mA
I2 7 0 20mA
I3 5 0 10mA
```

```
*ESD diodes
XD1 2000  101 0 HDE113032
XD2    0 2000 0 HDE113032
XD3 2001  101 0 HDE113032
XD4    0 2001 0 HDE113032

.ENDS INDRV
************************************************

************************************************
.SUBCKT INPKG 2101 2102 2000 2001

LP1 2101 2000 1.5N
LP2 2102 2001 1.5N
CP1 2101    0 .2pF
CP2 2000    0 .4pF
CP3 2102    0 .2pF
CP4 2001    0 .4pF

.ENDS INPKG
************************************************

************************************************
* Q1, Q2, Q5 and Q6 Transistor Model
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+   VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
************************************************

************************************************
* ESD Diode Model
.SUBCKT H11A05 1 2 3 21
CP1EPI 1 2 3.949F
CP1P2 12 3 6.473F
CTRENCH 1 20 8.610F
RBX 2 12 61.077 TC=2.649M
RCX 1 10 40.300 TC=2.883M,1.658U
RCI 10 11 2.121 TC=2.883M,1.658U
REX 13 3 8.656 TC=182.441U
RSUB 20 21 11.846K
```

```
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=1.151E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=44.016M
+   IKR=806.400U ISE=5.444E-021 ISC=7.000E-030 RB=61.077 RBM=45.808
+   IRB=7M CJE=37.151F MJE=490M VJE=940M FC=990M CJC=7.359F MJC=470M
+   VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=20.430M PTF=5 KF=1.500F
+   AF=1 )
.MODEL TXP PNP( IS=6.540E-019 CJE=7.359F MJE=470M VJE=850M CJC=9.940F
+   MJC=400M VJC=650M BF=10K BR=672.167U TF=1N FC=900M )
.ENDS H11A05
************************************************

.PROBE
.END
```