

MAX3676 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A0, August 25, 2004

I/O Models for the MAX3676

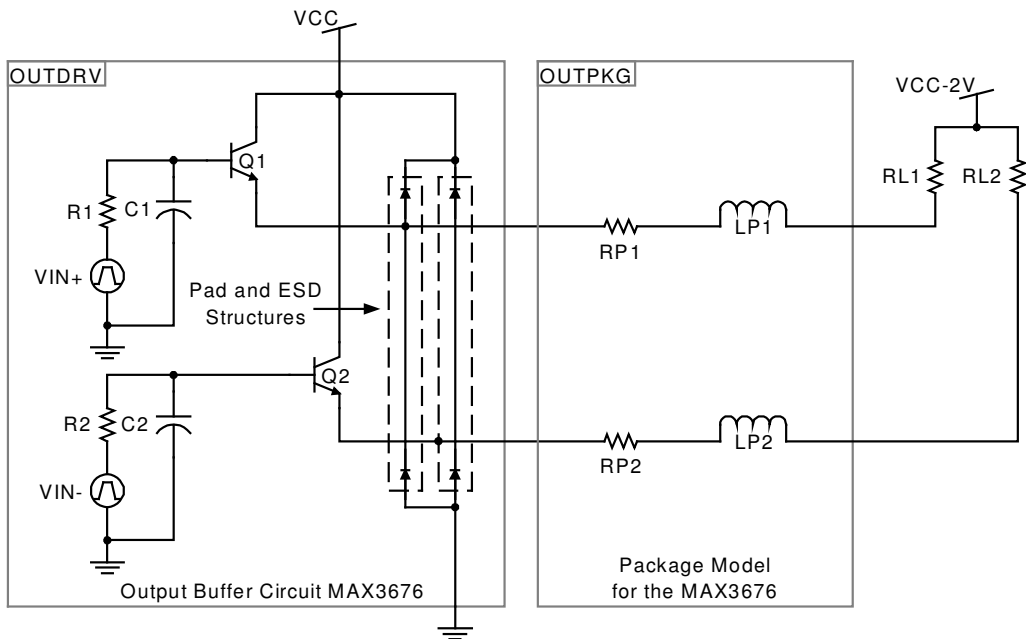


Figure 1. Output Model for signals SD0 and SCLK0 of the MAX3676.

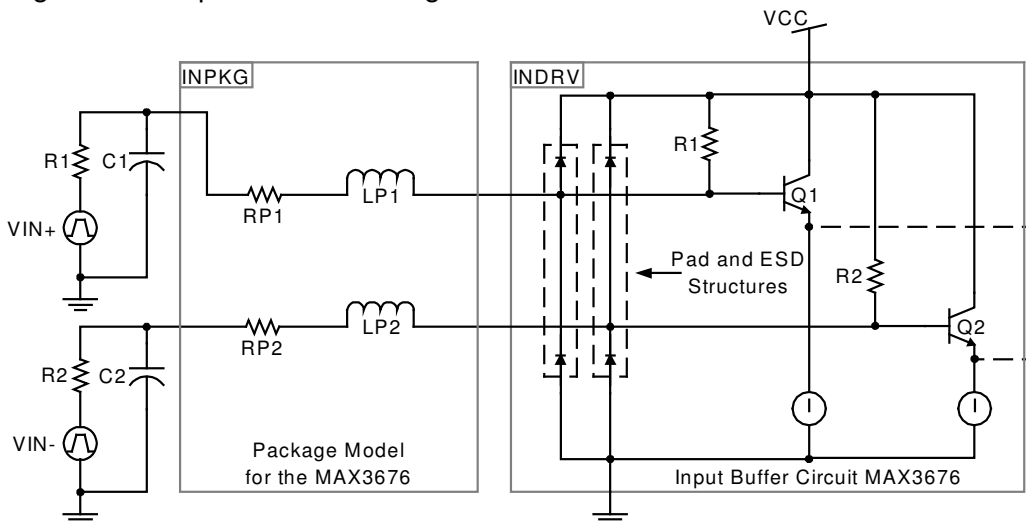


Figure 2. Input Model for signals ADI and DDI of the MAX3676.

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3676 622Mbps Clock Recovery and Data Retimer. The output circuit shown is for the signal outputs (SD0+, SCLK0+, SD0-, SCLK0-) and the input circuit is shown with the signal inputs (ADI+, DDI+, ADI-, DDI-). However, the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note the output signals are described as (2001, 2002) and the input signals are described as (2101, 2102). These models are only valid at 25°C. The bias currents for the input and output circuitry are modeled by ideal current sources. This model is not compensated for variations in VCC, so VCC equal to 3.3V should be used. The MAX3676 is sold in both dice and package format. The model is currently set up for having a package. To model the dice format, open both models, delete all references to OUTPKG and INPKG. The output model also needs to change the output resistors nodes to 50, 51 instead of 2001, 2002. For the input model you need to replace all instances of nodes 1001, 1002 to 2101, 2102.

The Output Stage: The output stage of the MAX3676 is shown as the sub-circuit “OUTDRV”.

The OUTDRV Sub-circuit: The driver sub-circuit is a simplified version of the output stage used by the MAX3676 CDR. The output signals are terminated with 50Ω resistors to VCC - 2V. This model is capable of setting a V_{OH} of 2.275V to 2.42V and a V_{OL} of 1.49V to 1.68V. To set the output voltage, you must set VINP and VINN to the correct values. See Table 1 for instructions. The waveform is a pulse whose period is 3.2ns with rise and fall times of approximately 180ps. The netlist is given in SPICE 2G6 format in Appendix A.

VINP	V_{OH}		VINN	V_{OL}
3.3V	2.42V	MAXIMUM	2.512	1.68V
3.226V	2.3475V	AVERAGE	2.407V	1.585V
3.147V	2.275V	MINIMUM	2.229	1.49V

The Input Stage: The input stage has the sub-circuit “INDRV”.

The INDRV Sub-circuit: The signal continues through the input buffer from nodes 1 and 2 (positive and negative nodes respectively). The input voltage should fit within certain parameters. V_{IH} should be in between 2.14V to 2.42V. V_{IL} should be in between 1.49V to 1.82V. See Appendix B for the input netlist.

Text File Format: This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file.

Appendix A: Output Netlist

* 3676 Output Model

.OPT ACCT NOMOD LIMPTS=10000

.TEMP 25

.OP

.TRAN 2P 10n

* Voltage Source

VCC 101 0 3.3

* VCC – 2V

VL 102 0 1.3

* Load Resistors

RL1 102 2001 50

RL2 102 2002 50

XOUTPKG 2001 2002 50 51 OUTPKG

XOUTDRV 50 51 101 OUTDRV

.SUBCKT OUTDRV 50 51 101

* For Maximum Output:

* VINP 1 0 PULSE (3.3 2.512 0.0n 180p 180p 1.5n 3.21543n)

* VINN 3 0 PULSE (2.512 3.3 0.0n 180p 180p 1.5n 3.21543n)

* For Minimum Output:

* VINP 1 0 PULSE (3.147 2.299 0.0n 180p 180p 1.5n 3.21543n)

* VINN 3 0 PULSE (2.299 3.147 0.0n 180p 180p 1.5n 3.21543n)

* For Average Output:

VINP 1 0 PULSE (3.226 2.407 0.0n 180p 180p 1.5n 3.21543n)

VINN 3 0 PULSE (2.407 3.226 0.0n 180p 180p 1.5n 3.21543n)

* Values to generate waveform

R1 2 1 50

R2 4 3 50

C1 2 0 1.9p

C2 4 0 1.9p

* Emitter Followers

XQ1 101 2 50 0 H14E062_4

XQ2 101 4 51 0 H14E062_4

* ESD Diodes
XD1 50 101 0 HDE113032
XD2 0 50 0 HDE113032
XD3 51 101 0 HDE113032
XD4 0 51 0 HDE113032

* Pad Structures
XP1 50 0 HPAD3
XP2 51 0 HPAD3

.ENDS OUTDRV

.SUBCKT OUTPKG 2001 2002 50 51

* For dice operation, remove all references to
* OUTPKG and change the nodes the load resistors
* connect too (50, 51 instead of 2001, 2002).

RP1 50 500 70M
RP2 51 501 70M
LP1 500 2001 1.6N
LP2 501 2002 1.6N

.ENDS OUTPKG

* Transistor Model

.SUBCKT H14E062_4 1 2 3 21

CP1EPI 1 2 74.690F

CP1P2 12 3 107.750F

CTRENCH 1 20 68.882F

RBX 2 12 3.920 TC=2.687M

RCX 1 10 4.297 TC=2.434M,1.079U

RCI 10 11 226.149M TC=2.434M,1.079U

REX 13 3 525.627M TC=69.810U

RSUB 20 21 1.196K

QP 20 10 12 20 TXP 4 OFF

QN 11 12 13 11 TX 4

.MODEL TX NPN(IS=4.094E-017 XTI=3 EG=1.140 BF=246.294 BR=20 XTB=450M

+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=154.056M

+ IKR=2.822M ISE=1.936E-020 ISC=2.489E-029 RB=15.681 RBM=11.761

+ IRB=24.895M CJE=133.480F MJE=490M VJE=940M FC=990M CJC=28.846F

+ MJC=470M VJC=850M TF=3.728P TR=19N XTF=1 VTF=1K ITF=74.440M PTF=5

+ KF=1.500F AF=1)

```
.MODEL TXP PNP( IS=2.640E-018 CJE=28.846F MJE=470M VJE=850M
CJC=35.172F
+ MJC=400M VJC=650M BF=10K BR=1.492M TF=1N FC=900M )
.ENDS H14E062_4
```

* Diode Model

```
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
```

* Pad Model

```
.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3
```

```
.PROBE
.END
```

Appendix B: Input Netlist

* 3676 Input Model

.OPT ACCT NOMOD LIMPTS=10000

.TEMP 25

.OP

.TRAN 2P 10n

* Voltage Source

VCC 101 0 3.3V

* Add input source here.

* The source should connect to node 2101 (VINP)

* and 2102 (VINN).

* Example:

VINP 50 0 PULSE (2.28 1.655 0.04n 180p 180p 1.5n 3.21543n)

VINN 60 0 PULSE (1.655 2.28 0.04n 180p 180p 1.5n 3.21543n)

R1 2101 50 50

R2 2102 60 50

C1 2101 0 4.7p

C2 2102 0 4.7p

XINPKG 2101 2102 1000 1001 INPKG

XINDRV 1000 1001 101 INDRV

.SUBCKT INDRV 1000 1001 101

* Input Terminating Resistors

R3 101 1000 50

R4 101 1001 50

* Emitter Followers

XQ1 101 1000 1 0 H11M02

XQ2 101 1001 2 0 H11M02

* Current Sources

I1 1 0 .2mA

I2 2 0 .2mA

* ESD Diodes
XD1 1000 101 0 HDE113032
XD2 0 1000 0 HDE113032
XD3 1001 101 0 HDE113032
XD4 0 1001 0 HDE113032

* Pad Structures
XP1 1000 0 HPAD3
XP2 1001 0 HPAD3

.ENDS INDRV

.SUBCKT INPKG 2101 2102 1000 1001

* For dice operating, remove all references to INPKG and
* change nodes 1001, 1002, to 2101, 2102.

RP1 1000 2002 70M
RP2 1001 2003 70M
LP1 2002 2101 1.6N
LP2 2003 2102 1.6N

.ENDS INPKG

* Transistor Models

.SUBCKT H11M02 1 2 3 21

CP1EPI 1 2 9.985E-016

CP1P2 12 3 1.848F

CTRENCH 1 20 4.783F

RBX 2 12 271.456 TC=2.588M

RCX 1 10 186.577 TC=3.250M,2.039U

RCI 10 11 9.820 TC=3.250M,2.039U

REX 13 3 39.087 TC=44.406U

RSUB 20 21 26.178K

QP 20 10 12 20 TXP OFF

QN 11 12 13 11 TX

.MODEL TX NPN(IS=1.920E-018 XTI=3 EG=1.140 BF=265 BR=20 XTB=450M

VAF=29

+ VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=6.878M IKR=126U

+ ISE=9.083E-022 ISC=1.168E-030 RB=271.456 RBM=203.592 IRB=1.168M

+ CJE=6.452F MJE=490M VJE=940M FC=990M CJC=1.729F MJC=470M

VJC=850M

+ TF=3.651P TR=19N XTF=1 VTF=1K ITF=3.568M PTF=5 KF=1.500F AF=1)


```
.MODEL TXP PNP( IS=1.680E-019 CJE=1.729F MJE=470M VJE=850M CJC=3.870F
+ MJC=400M VJC=650M BF=10K BR=664.767U TF=1N FC=900M )
.ENDS H11M02
```

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*****
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*****
```

```
* Pad Model
```

```
.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M,5U
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3
```

```
*****
```

```
*****
```

```
* Diode Model
```

```
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
```

```
*****
```

```
.PROBE
.END
```