MAX3665 Output Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Component*s.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

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Output Model for the MAX3665

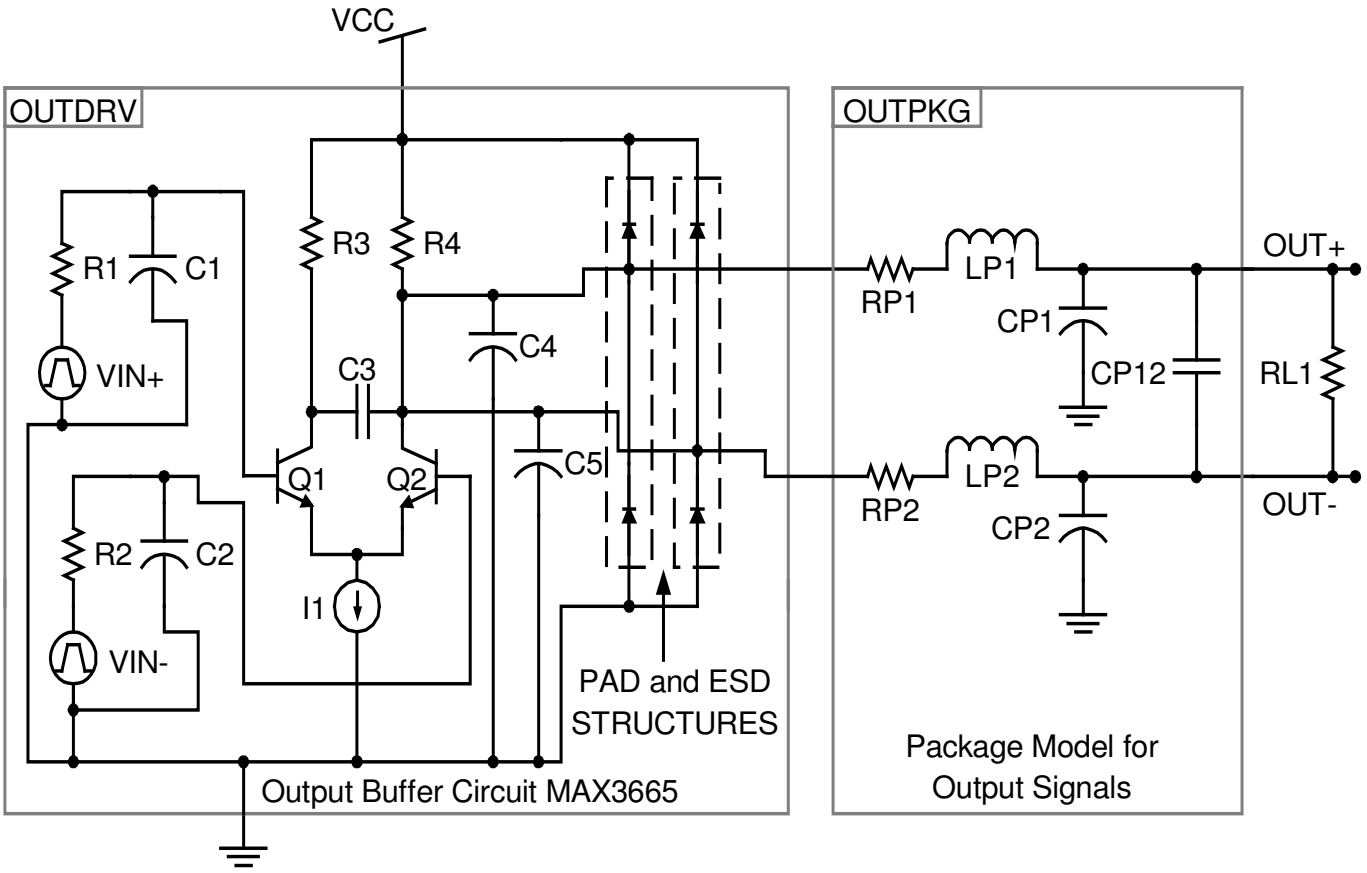

Figure 1. Output model for the MAX3665.

Notes:

The schematics on the previous page represent the output stage of the Maxim MAX3665 622Mbps Transimpedance Preamplifier. The output circuit shown is for the signal outputs (OUT+, OUT-). However the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note, the output signals are described as (2001, 2002). This model is only valid at 25°C. The bias current for the output circuitry is modeled by an ideal current source. This model is compensated for variations in VCC, so VCC equal to 3.3V or 5V should be used. ESD and PAD structures have been modeled. The package model has had all of the parasitic components calculated.

The Output Stage: The output stage of the MAX3665 is shown as the sub-circuit "OUTDRV".

The OUTDRV Sub-circuit: The outdrv sub-circuit is a simplified version of the output stage used by the MAX3665 Transimpedance Preamplifier. The output stage is driven by a differential amplifier and terminated differentially with 100Ω. Each side of the differential pair is composed of two H14E04 NPN bipolar transistors in parallel with each other. Usually a 50Ω transmission line connects the output stage to a low pass filter. The filter is then connected to .1uF coupling capacitors, which connects to the inputs of a limiting amplifier. See Figure 3 in the MAX3665 data sheet on how to design the low pass filter. The output waveform is configured to be at a differential voltage of 260mV peak to peak. The output common mode voltage has been set to 3.16V. The output waveform has a frequency of 311Mhz. In Appendix A, the netlist is given in SPICE 2G6 format.

Text File Format: This model is shipped in "pdf" format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the "Text Select Tool." Then the user can "select" what netlist and/or subcircuit with the mouse. Then use the copy command from the "edit" menu to capture the selected lines. These lines can then be "pasted" into the user's text file.

Appendix A: Output Netlist

```
* 3665 Output Model
**********************************************
.OPT ACCT NOMOD LIMPTS=10000
.TEMP 25
.OP
.TRAN 2P 4n
**********************************************

* Voltage Source (VCC)
VCC 101 0 3.3
* Differential Output Resistance (100 ohms)
RL1 2001 2002 100

**********************************************
XOUTPKG 2001 2002 50 51 OUTPKG
XOUTDRV 50 51 101 OUTDRV
**********************************************

**********************************************
.SUBCKT OUTDRV 50 51 101

VINP 1  0 PULSE (1 1.5 0n 0.20n 0.20n 1.47n 3.30325n)
VINN 3  0 PULSE (1.5 1 0n 0.20n 0.20n 1.47n 3.30325n)
R1 2 1 50
R2 4 3 50
C1 2 0 12.5p
C2 4 0 12.5p

* Differential Pair
XQ1 50 2 5 0 H14E04_2
XQ2 51 4 5 0 H14E04_2

* Biasing Current
I1 5 0 5.335m

R3 101 50 50
R4 101 51 50

* Offset Capacitors
C3 50 51 1.2p
C4 50 0 10p
C5 51 0 10p

* ESD Structures
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```
XD1 50 101 0 HDE381011
XD2  0  50 0 HDE381011
XD3 101 51 0 HDE381011
XD4  0  51 0 HDE381011
* PAD structures
XP1 50 0 pad3
XP2 51 0 pad3

.ENDS OUTDRV
************************************************

************************************************
.SUBCKT OUTPKG 2001 2002 50 51

* Calculated package parameters
RP1    50   60 .0399
RP2    51   61 .0399
LP1    60 2001 1.446n
LP2    61 2002 1.455n
CP1  2001    0 .254p
CP2  2002    0 .193p
CP12 2001 2002 .061p

.ENDS OUTPKG
************************************************

************************************************
* Q1 and Q2 transistor models
.SUBCKT H14E04_2 1 2 3 21
CP1EPI 1 2 24.369F
CP1P2 12 3 39.268F
CTRENCH 1 20 30.614F
RBX 2 12 10.277 TC=2.663M
RCX 1 10 11.754 TC=2.354M,979.573N
RCI 10 11 618.650M TC=2.354M,979.573N
REX 13 3 1.397 TC=123.150U
RSUB 20 21 3.098K
QP 20 10 12 20 TXP 2 OFF
QN 11 12 13 11 TX 2
.MODEL TX NPN( IS=3.326E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=126.546M
+   IKR=2.318M ISE=1.573E-020 ISC=2.022E-029 RB=20.554 RBM=15.416
+   IRB=20.223M CJE=107.672F MJE=490M VJE=940M FC=990M CJC=21.929F
+   MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=59.621M PTF=5
+   KF=1.500F AF=1 )
```

```
.MODEL TXP PNP( IS=1.968E-018 CJE=21.929F MJE=470M VJE=850M
CJC=21.582F
+   MJC=400M VJC=650M BF=10K BR=809.067U TF=1N FC=900M )
.ENDS H14E04_2
************************************************

************************************************
* ESD Diode Models
.SUBCKT HDE381011 1 2 21
CP1EPI 1 4 79.338F
QD 5 4 1 5 QESD
RS 4 2 2.385 TC=3.113M,2.489U
RSUB 5 21 2.318K
CTRENCH 2 5 40.181F
.MODEL QESD PNP( IS=9.707E-018 NF=1.050 BF=800M BR=600U CJE=127.405F
+   VJE=600M MJE=400M CJC=64.825F VJC=650M MJC=400M )
.ENDS HDE381011
************************************************

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* PAD Models
.SUBCKT PAD3 1 3
CPAD 1 10 87.228F
REPI 10 20 250.111M TC=4.800M,5U
CTRENCH 21 20 22.394F
DS 21 20 DSUB
RS 3 21 369.115
.MODEL DSUB D( IS=12.656F CJO=885.938F M=500M VJ=450M )
.ENDS PAD3
************************************************

.PRINT TRAN V(2001) V(2002)
.PROBE
.END
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