MAX3787 Input/Output Model

SPICE I/O and Functional Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for HSPICE only as certain portions of the netlist are encrypted.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

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Maxim Integrated Products

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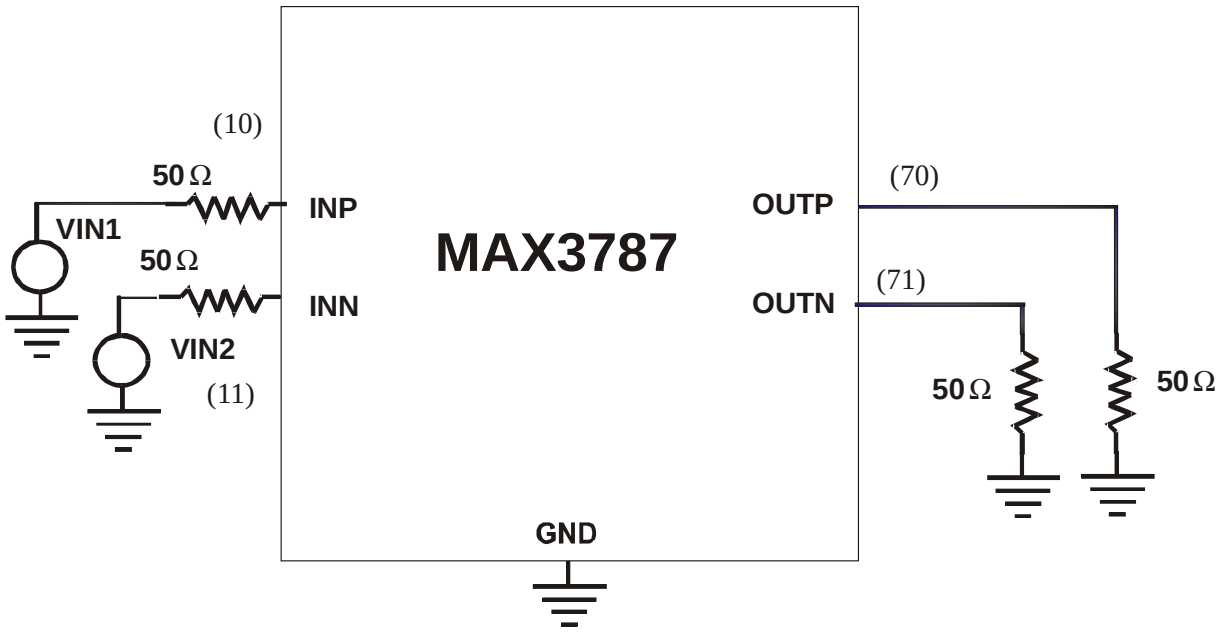

Figure 1. A schematic of the MAX3787 Input/Output model.

Notes:

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1) A circuit description of the input and output network reveals propriety information. As an alternative, the model provided is a s-parameter model. This model is based on experimental measurements of a MAX3787 device.
2) Since this model is passive, there is one model to provide information for both the input and output. This model will also provide the through response.
3) The functional netlist is included in this document and is accompanied by a Citifile called MAX3787.cit which are the s-parameter measurements. Note in the circuit netlist, the Citifile is referenced in a directory C:\CITIFILES\MAX3787.cit. If you do not have this file, you can get it by contacting Fiber Applications Group (503-547-2400) and requesting it.
4) This functional model is restricted to showing signal processing at room temperature and nominal process only.
5) This model generates roughly 250ps latency delay while the actual part has about 50ps delay.

Equalizer NETLIST:

MAX3787 Equalizer

* Input signal is 1 Vpeak for AC analysis

```
VPULA 201 0 PULSE(-0.4 +0.4 1ps 40p 40p 320p 800p)
E02 2 0 201 0 1.0
E03 3 0 201 0 -1.0

RINP 10 2 50
RINN 11 3 50
R1K28 1 0 100

ROUTP 70 0 50
ROUTN 71 0 50

EOUT 80 0 71 70 1

******** BEGINNING OF CIRCUIT   ****************************************

SSUB 10 11 70 71 0 mname=s4P

.MODEL s4p S n=4 citifile='c:\citifiles\MAX3787.cit' TYPE=S Zo=50  fmax=10e9

******** END OF CIRCUIT **********************************************

.tran 10p 4n
.AC dec 100 1GHZ 10000MEG
.PROBE
.END
```