

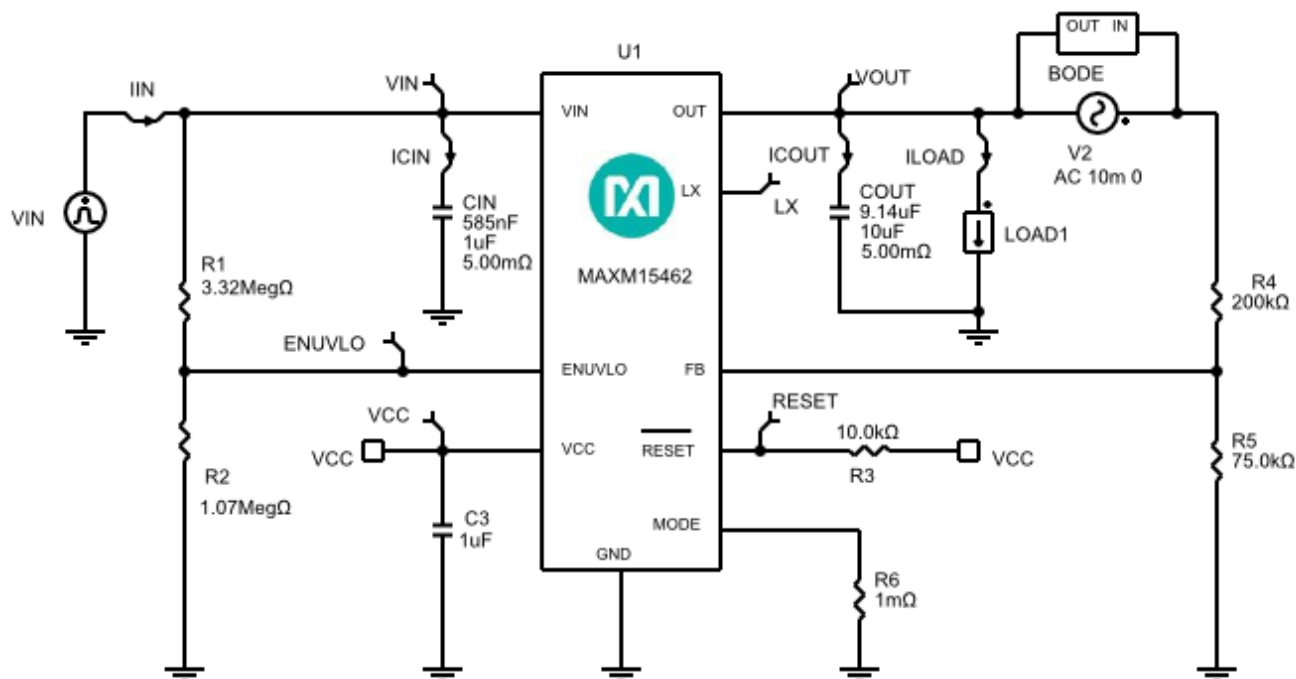
Initial Design

1.0

Design Requirements

Parameter	Value
Minimum Input Voltage	5.5V
Maximum Input Voltage	42V
Nominal Input Voltage	24V
Input Steady-State Ripple	5%
Input Undervoltage Lockout Level	4.95V
Output Voltage	3.3V
Load Current	0.3A
Mode of Operation	PWM
Switching Frequency	500kHz
Ambient Temperature	25°C
Soft Start time	4ms

Schematic



BOM

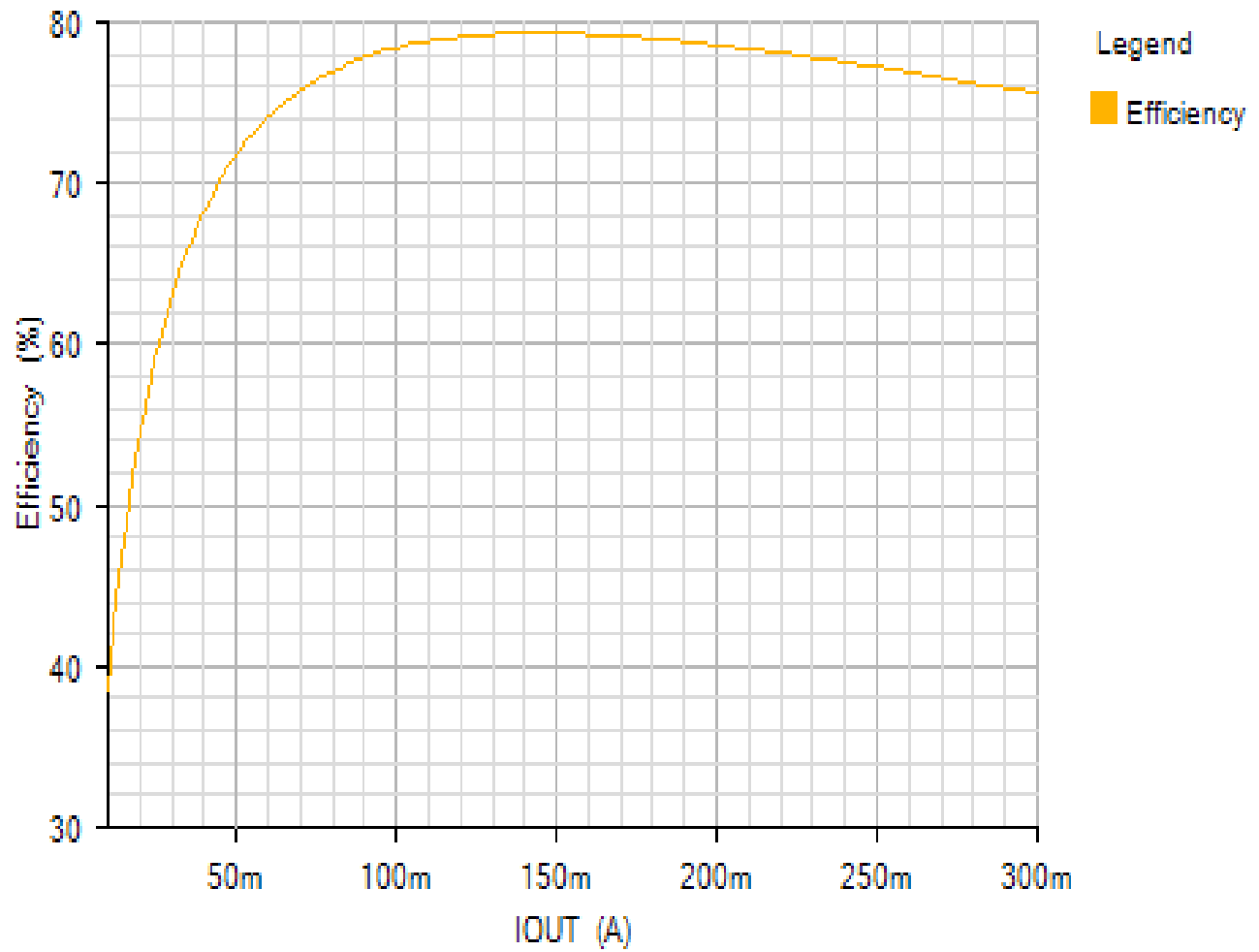
Ref	Qty	Part Number	Manufacturer	Description
U1	1	MAXM15462	User-Defined	IC
C3	1	CC0603KRX7R6BB105	Yageo	Cap Ceramic 1uF 10V X7R 10% Pad SMD 0603 125°C T/R
CIN	1	GRM21BR71H105KA12	Murata	Cap Ceramic 1uF 50V 0805 125C
COUT	1	C1206C106K9RAC	Kemet	Cap Ceramic 10uF 6.3V X7R 10% SMD 1206 125C Bulk
R1	1	RC0402FR-073M32L	Yageo	Res Thick Film 0402 3.32M Ohm 1% 0.063W(1/16W) ±100ppm/°C Epoxy Pad SMD T/R
R2	1	CRCW04021M07FKED	Vishay	Res Thick Film 0402 1.07M Ohm 1% 0.063W(1/16W) ±100ppm/°C Pad SMD Automotive T/R
R3	1	ERJ2RKF1002X	Panasonic	Res Thick Film 0402 10K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
R4	1	ERJ2RKF2003X	Panasonic	Res Thick Film 0402 200K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
R5	1	ERJ2RKF7502X	Panasonic	Res Thick Film 0402 75K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R

Simulation Results

Efficiency - Mon Jan 07 2019 10:28:36

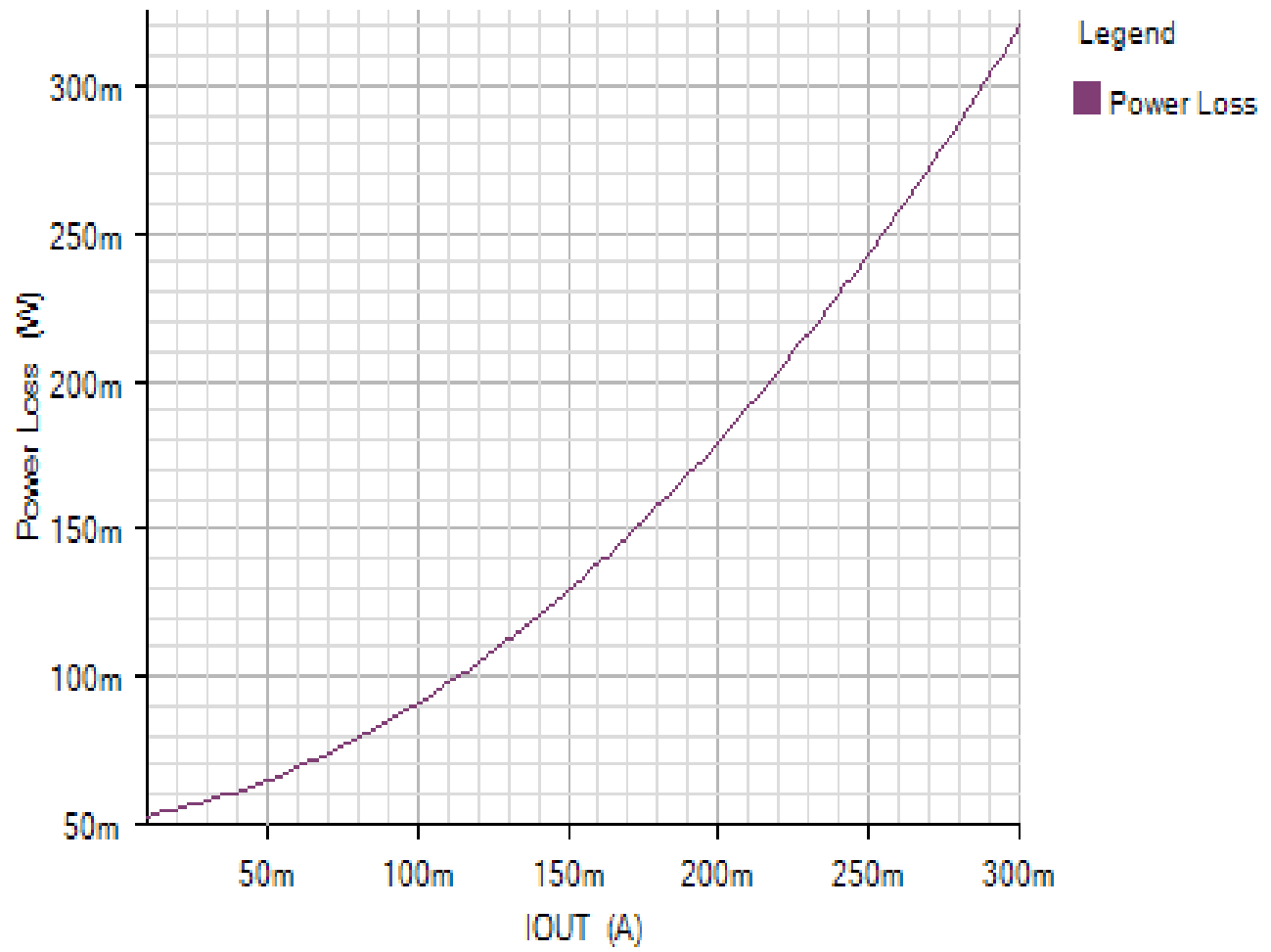
EFFICIENCY_PLOT

Default



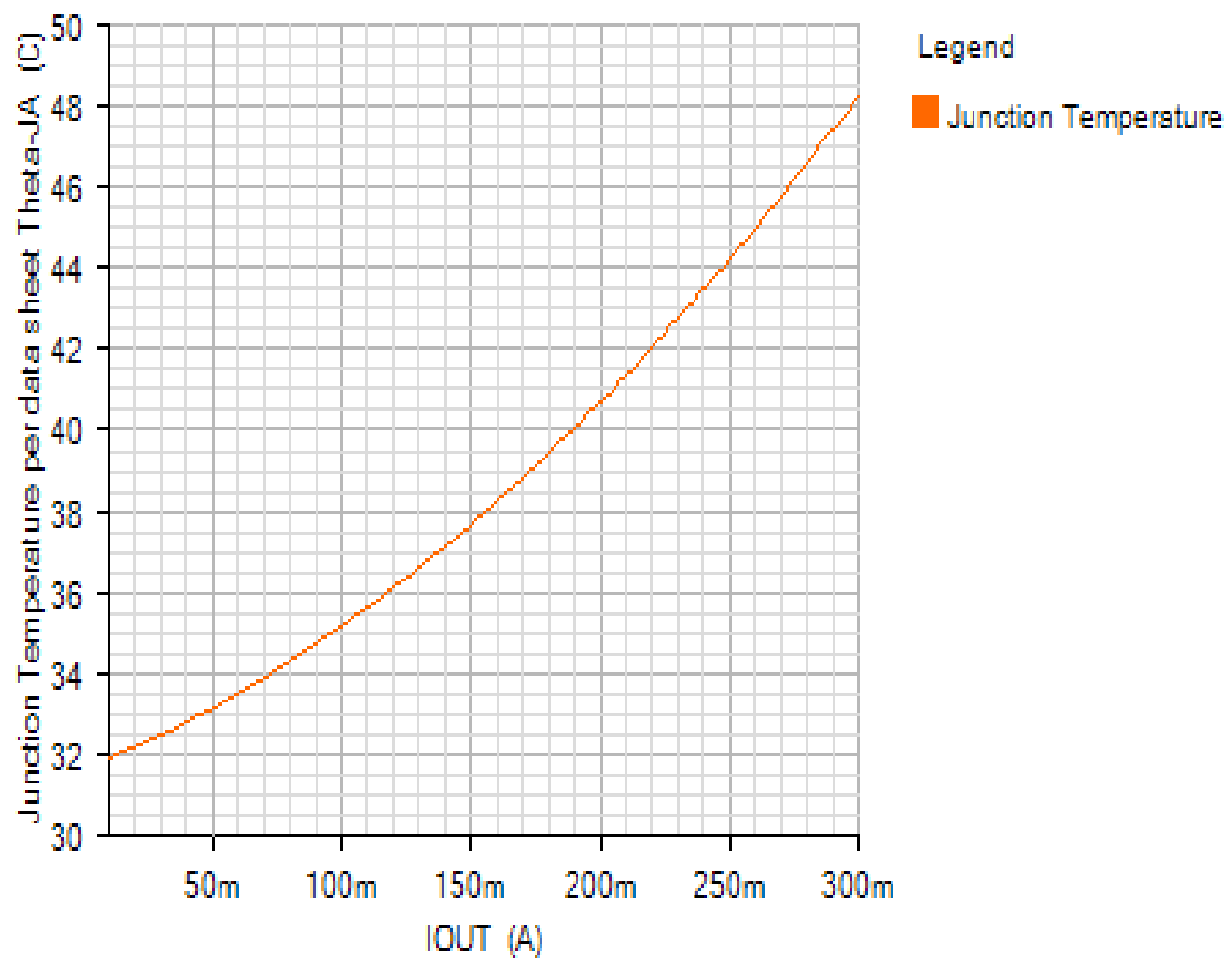
POWER_LOSS_PLOT

Default



JUNCTION_TEMPERATURE_PLOT

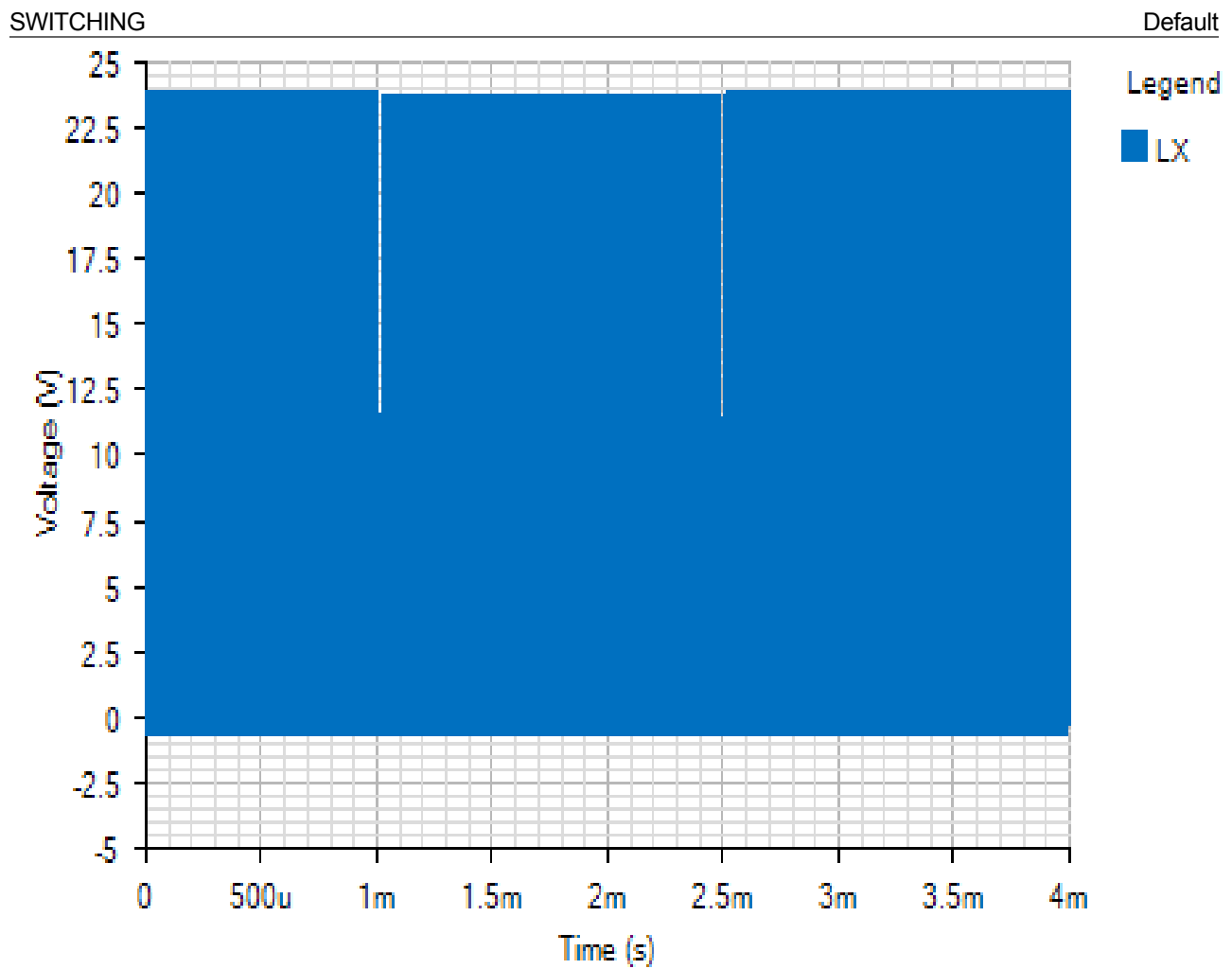
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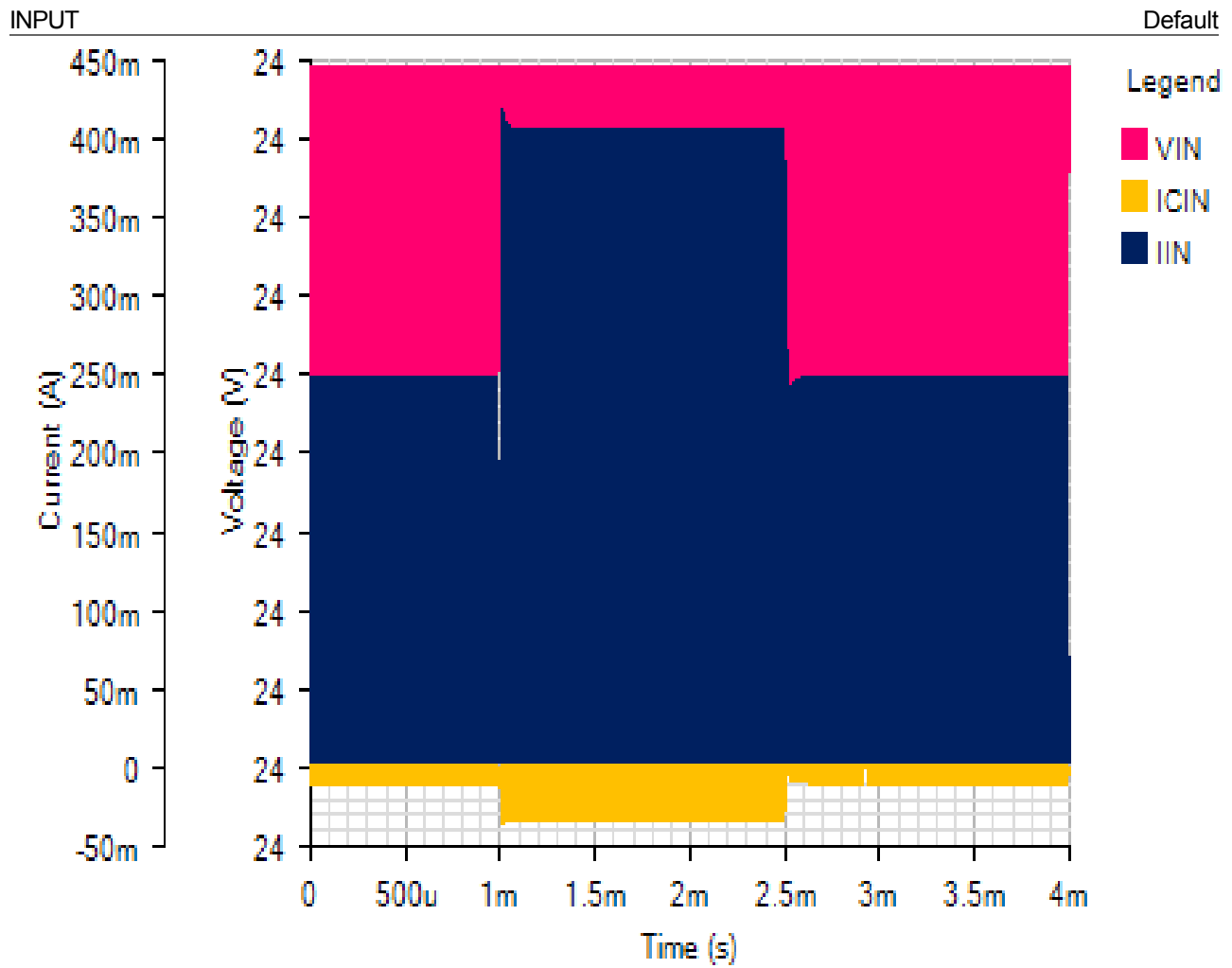


Losses

Component	Loss (W)	% of total
Total	0	100

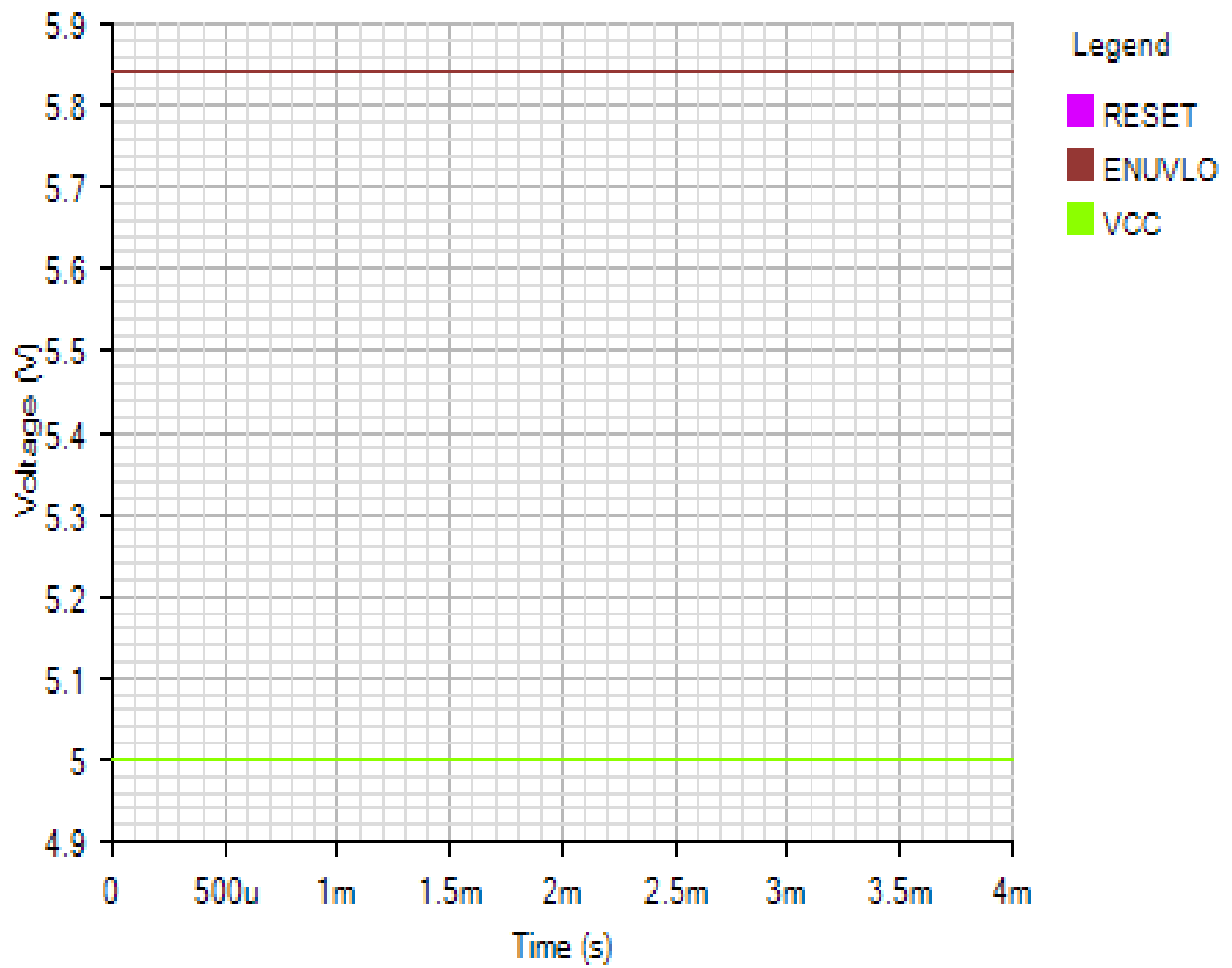
Load step - Mon Jan 07 2019 10:28:36





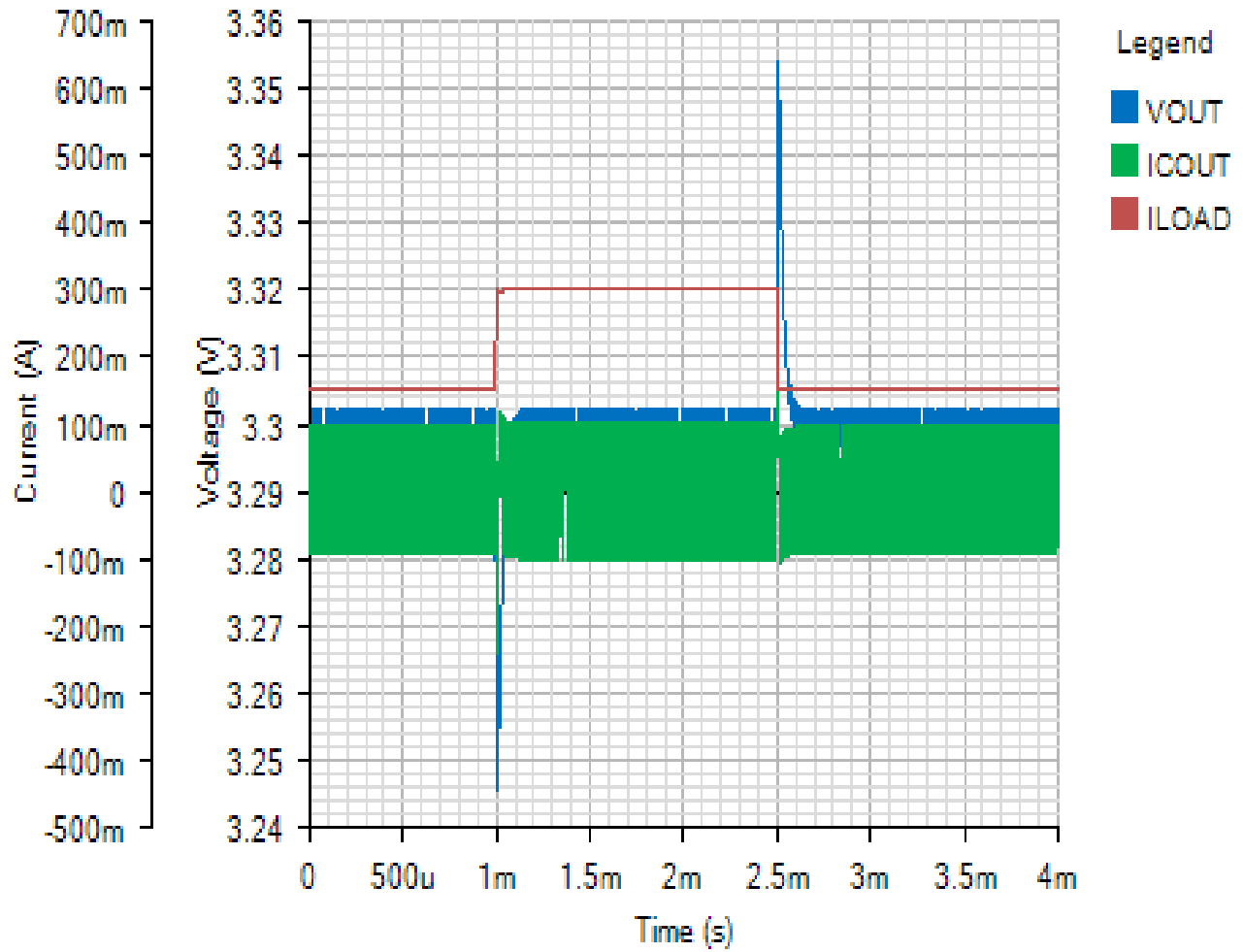
IC

Default



OUTPUT

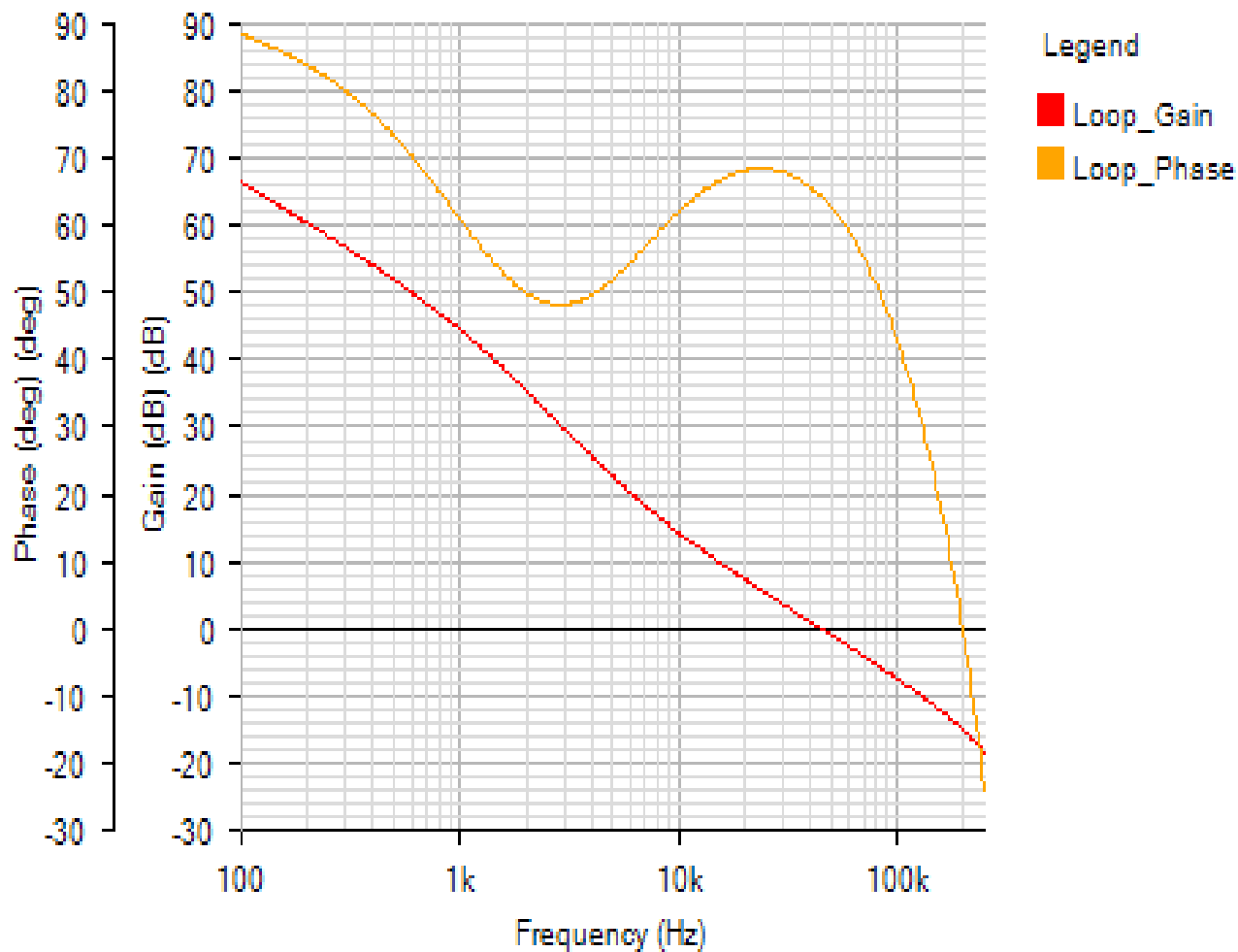
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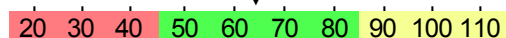
AC Loop - Mon Jan 07 2019 10:28:36

BODE

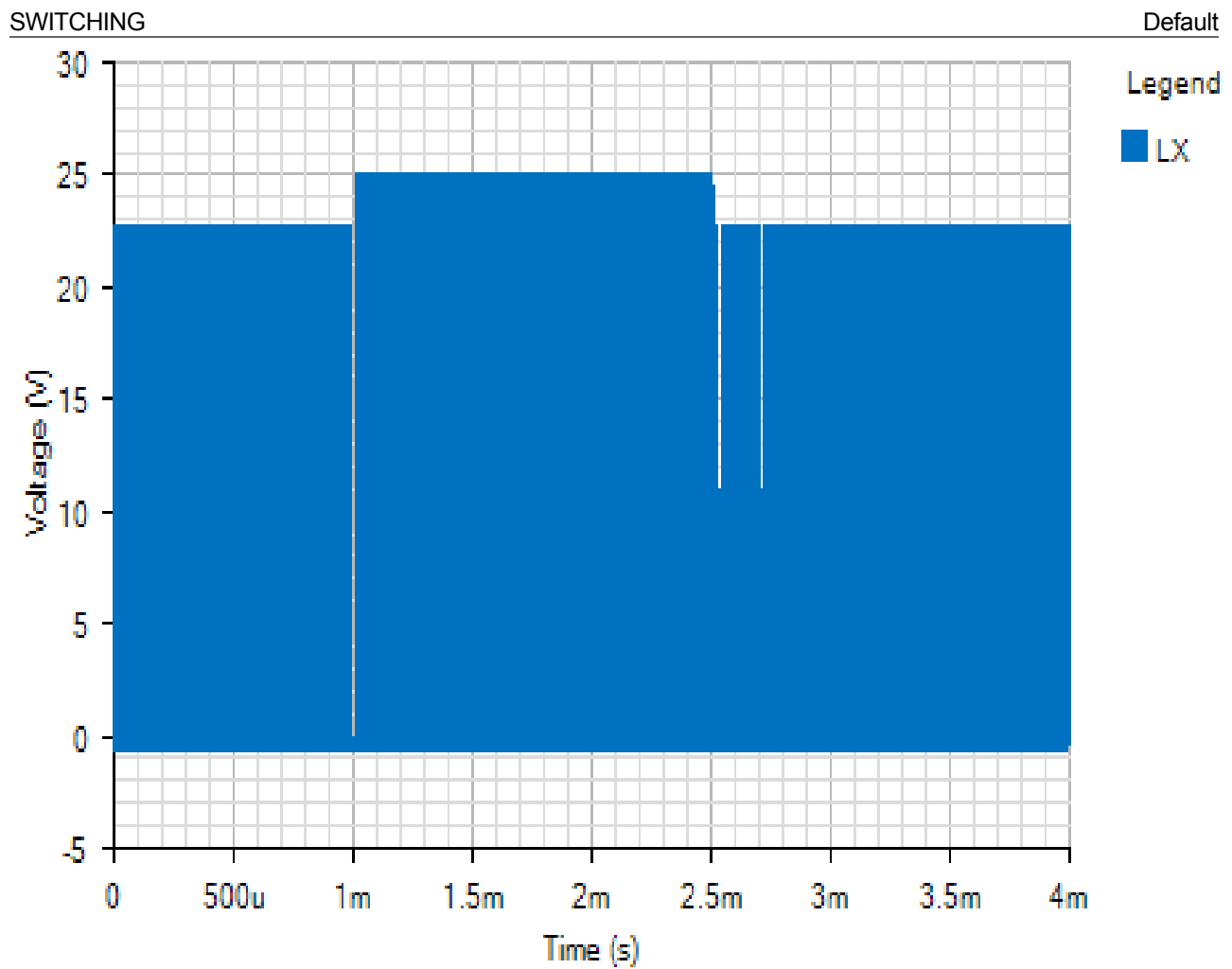
Default



Phase Margin: 64.36° at a crossover frequency of 44.7kHz

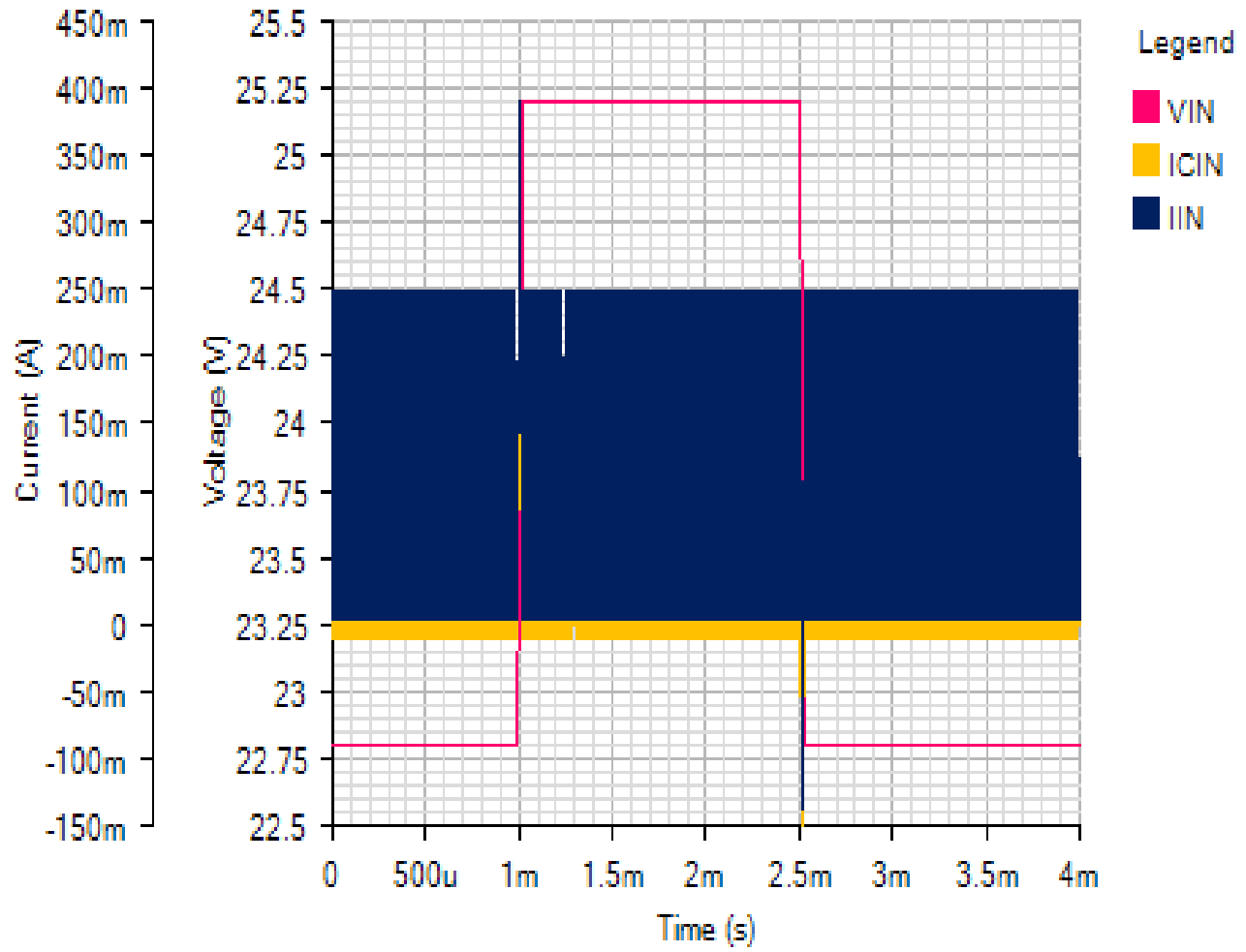


Line Transient - Mon Jan 07 2019 10:28:36



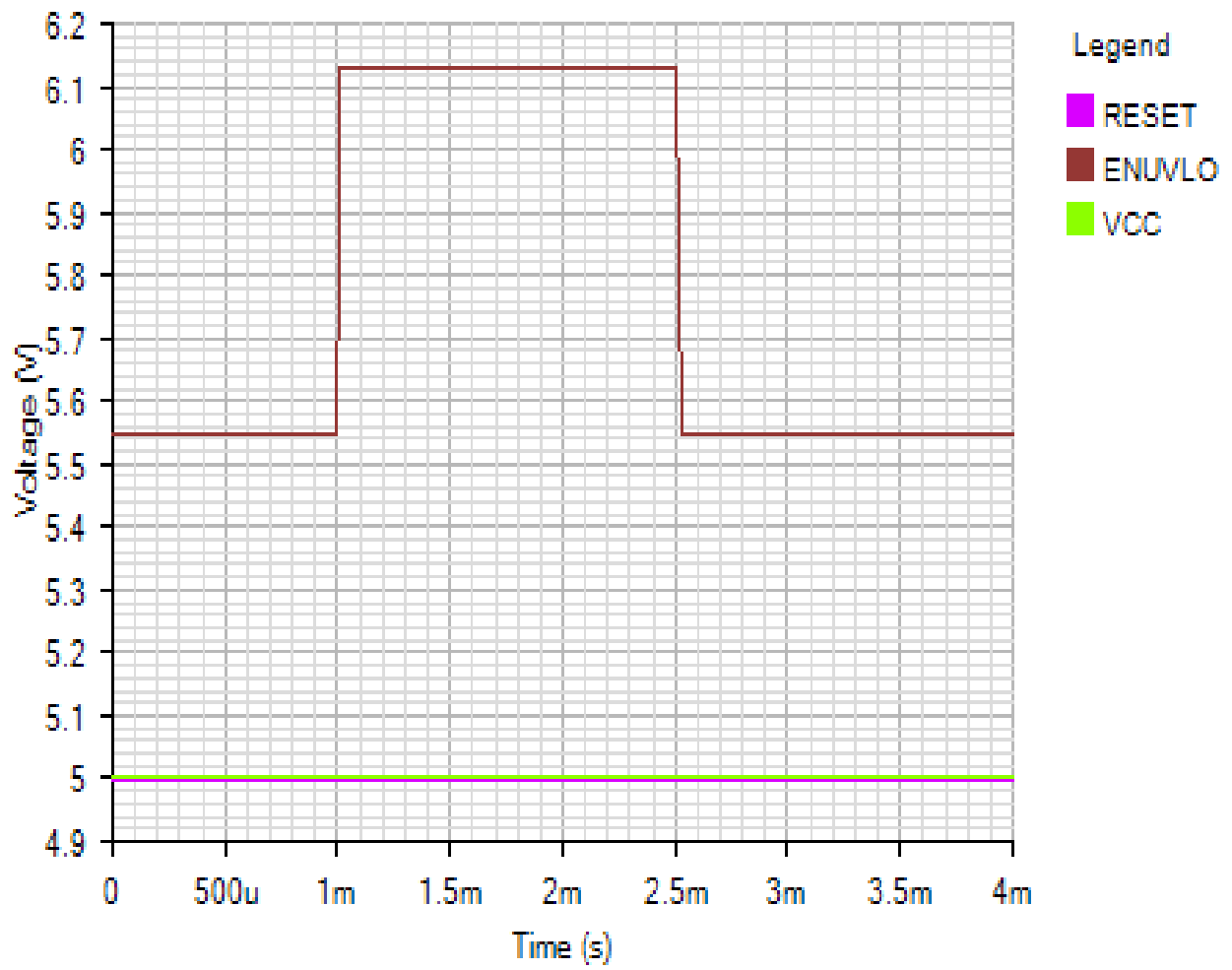
INPUT

Default



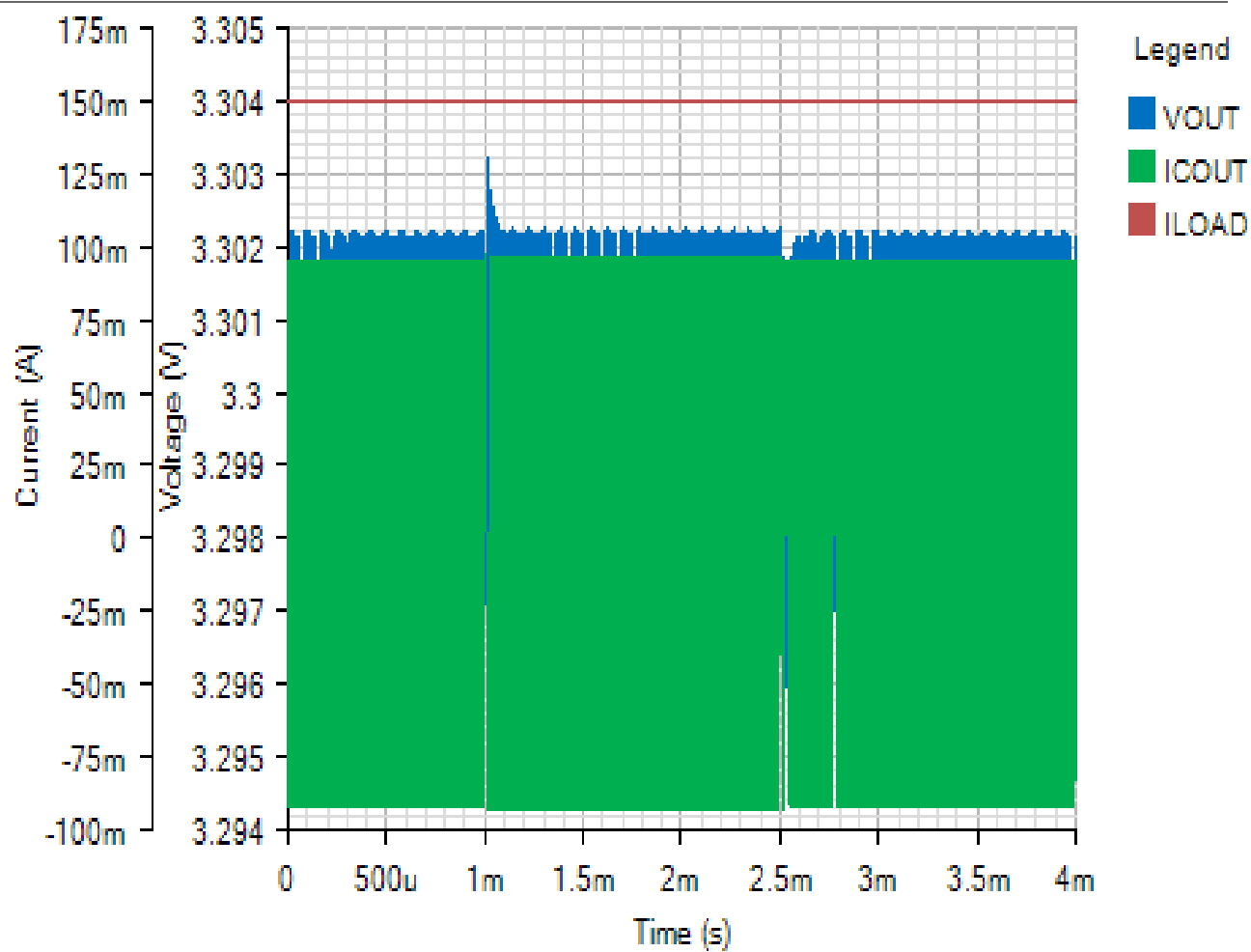
IC

Default



OUTPUT

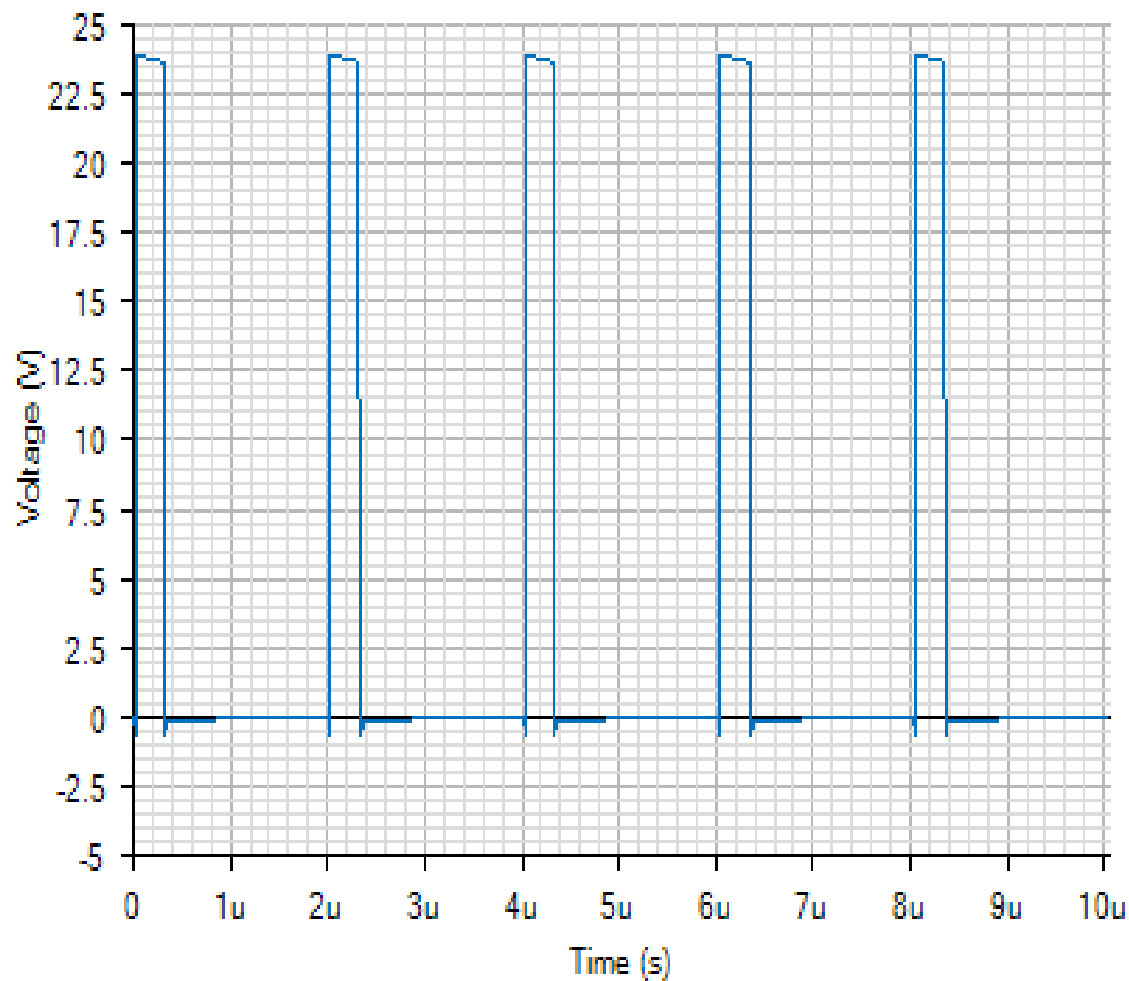
Default



Steady state - Mon Jan 07 2019 10:28:36

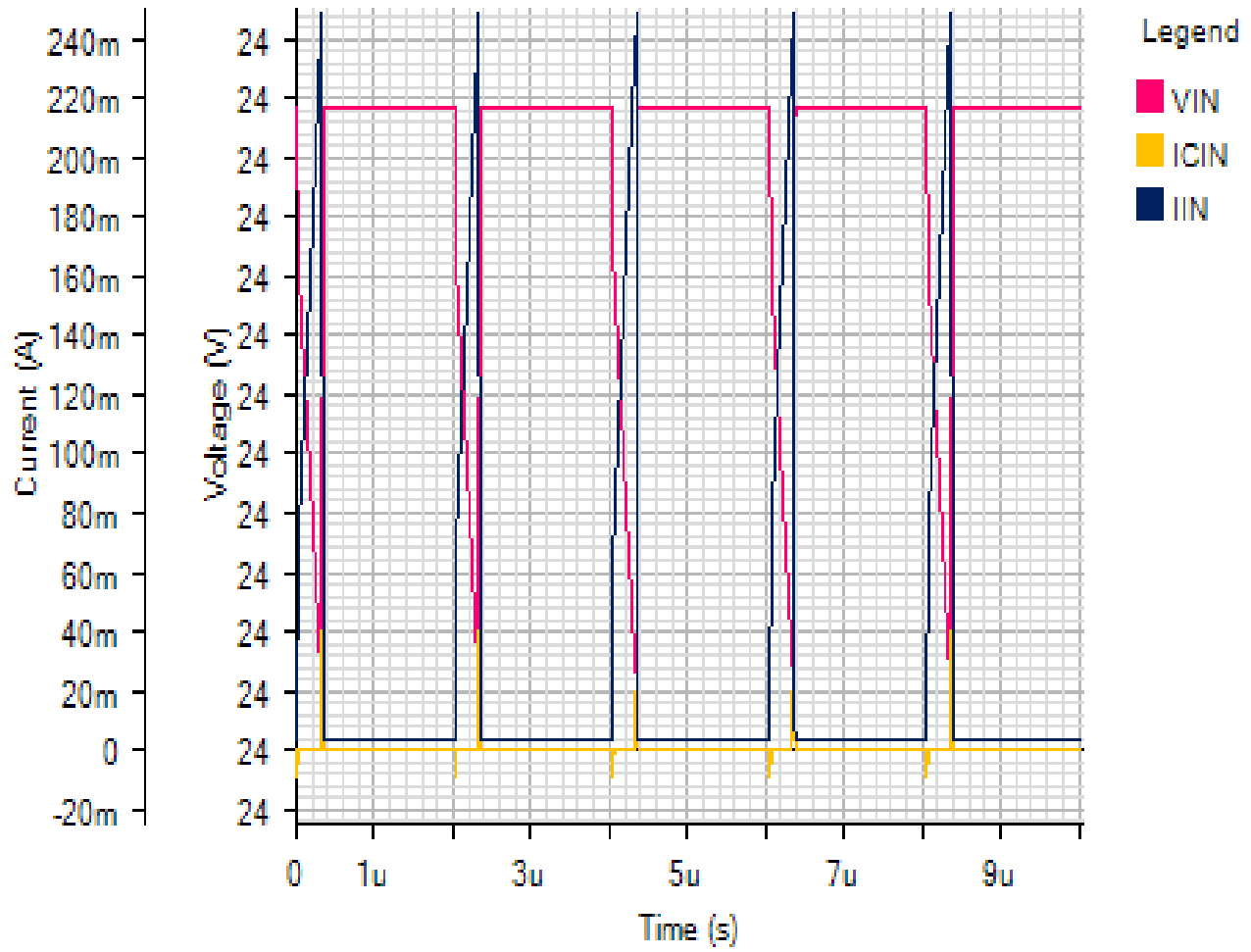
SWITCHING

Default



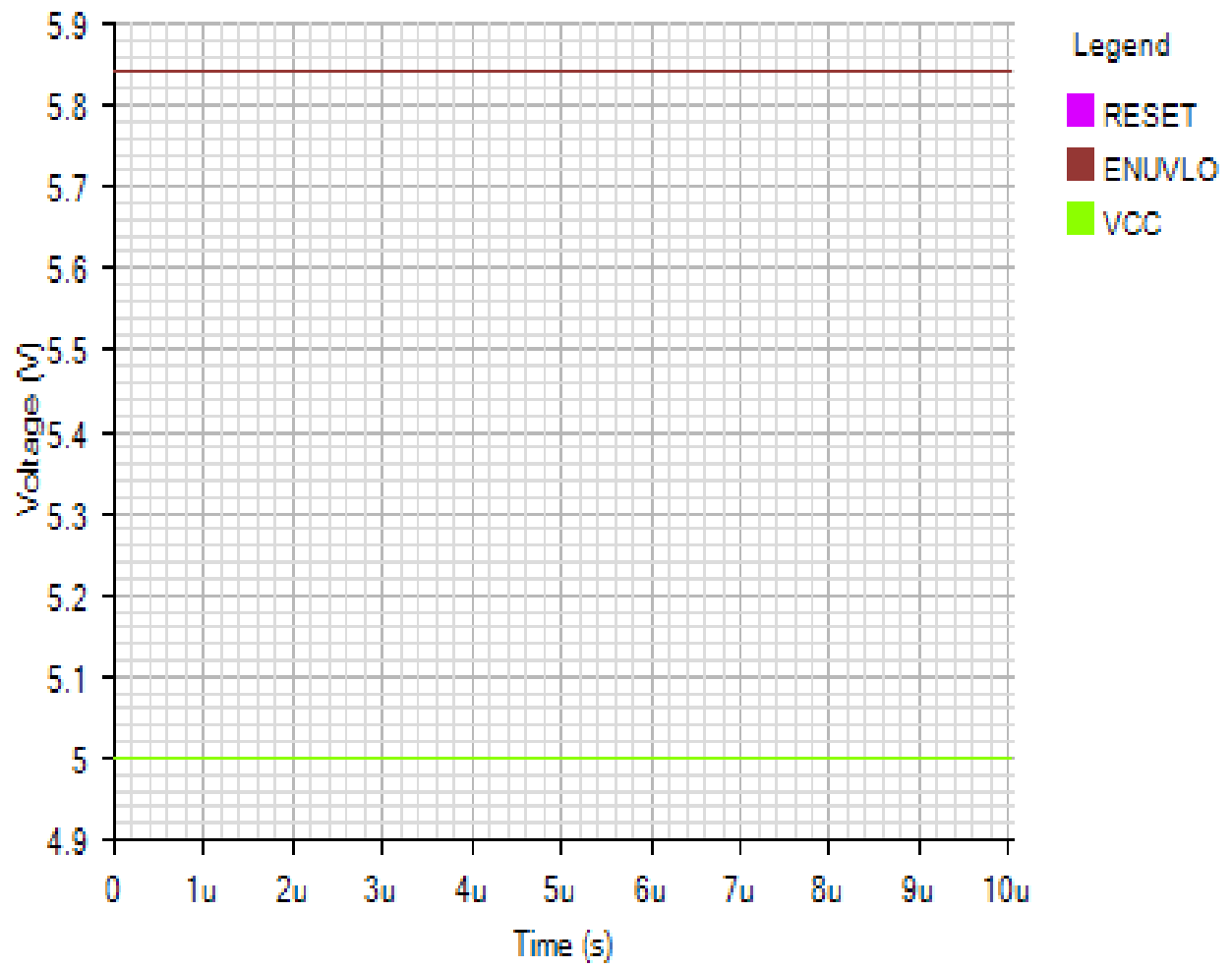
INPUT

Default



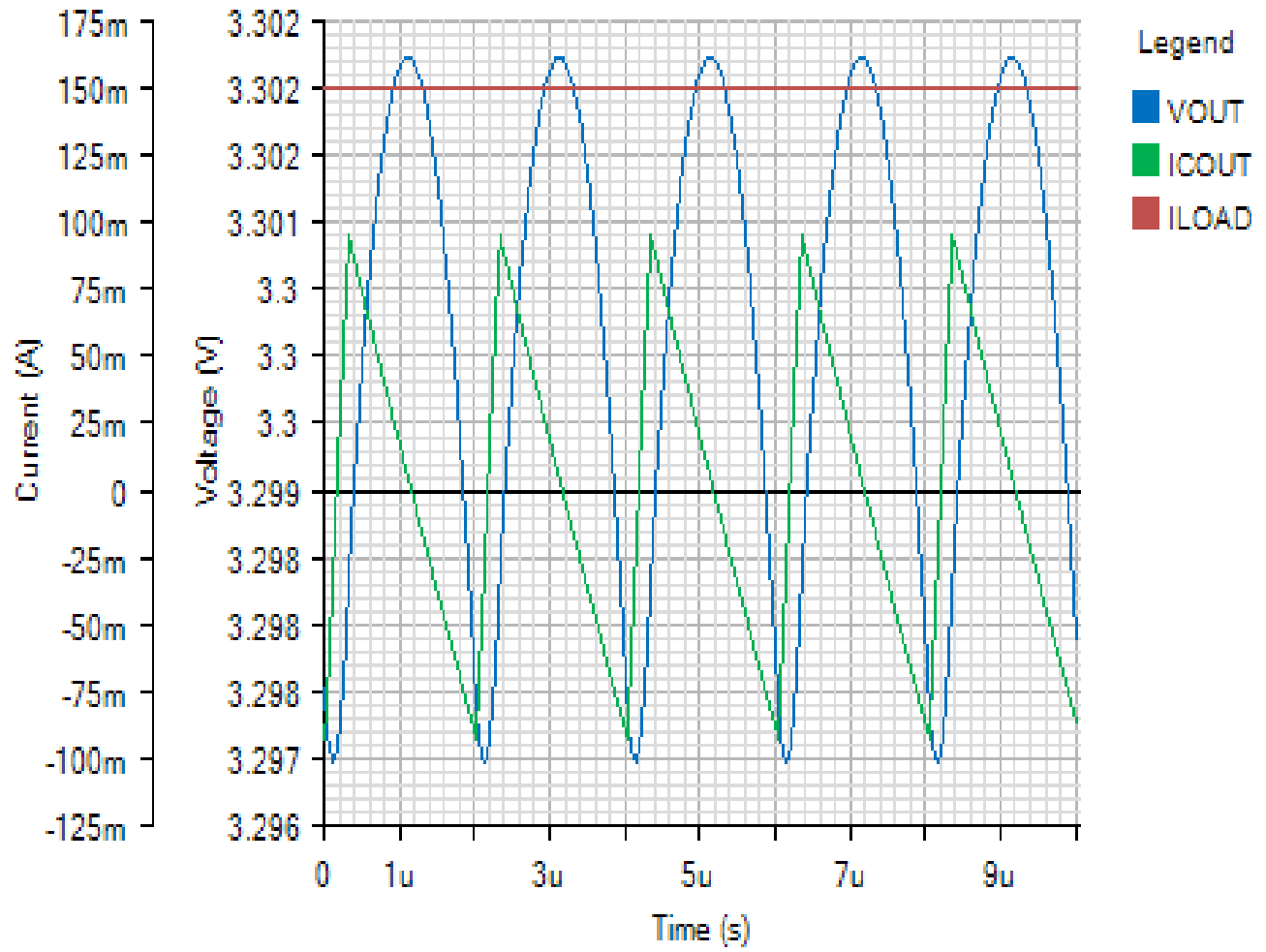
IC

Default

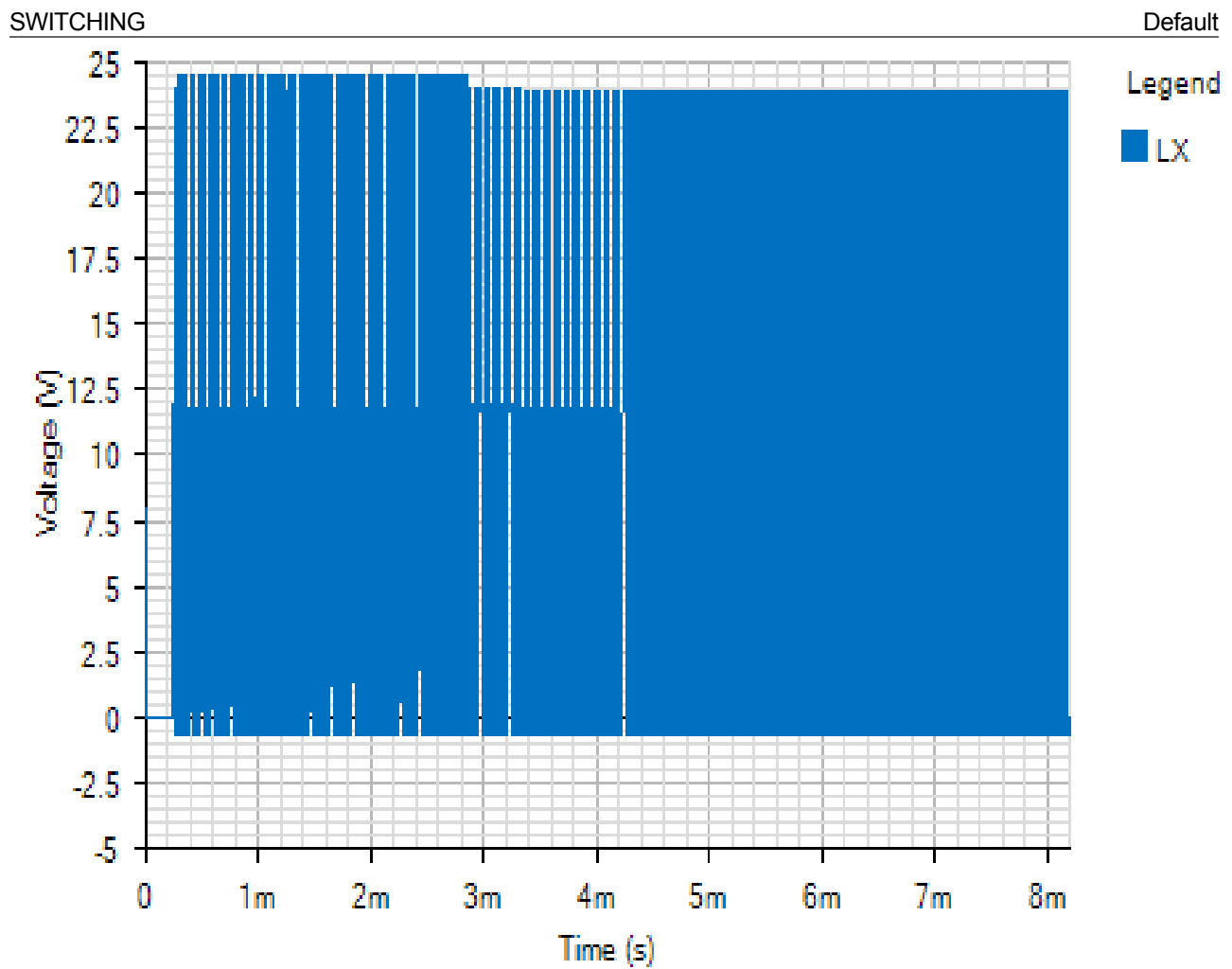


OUTPUT

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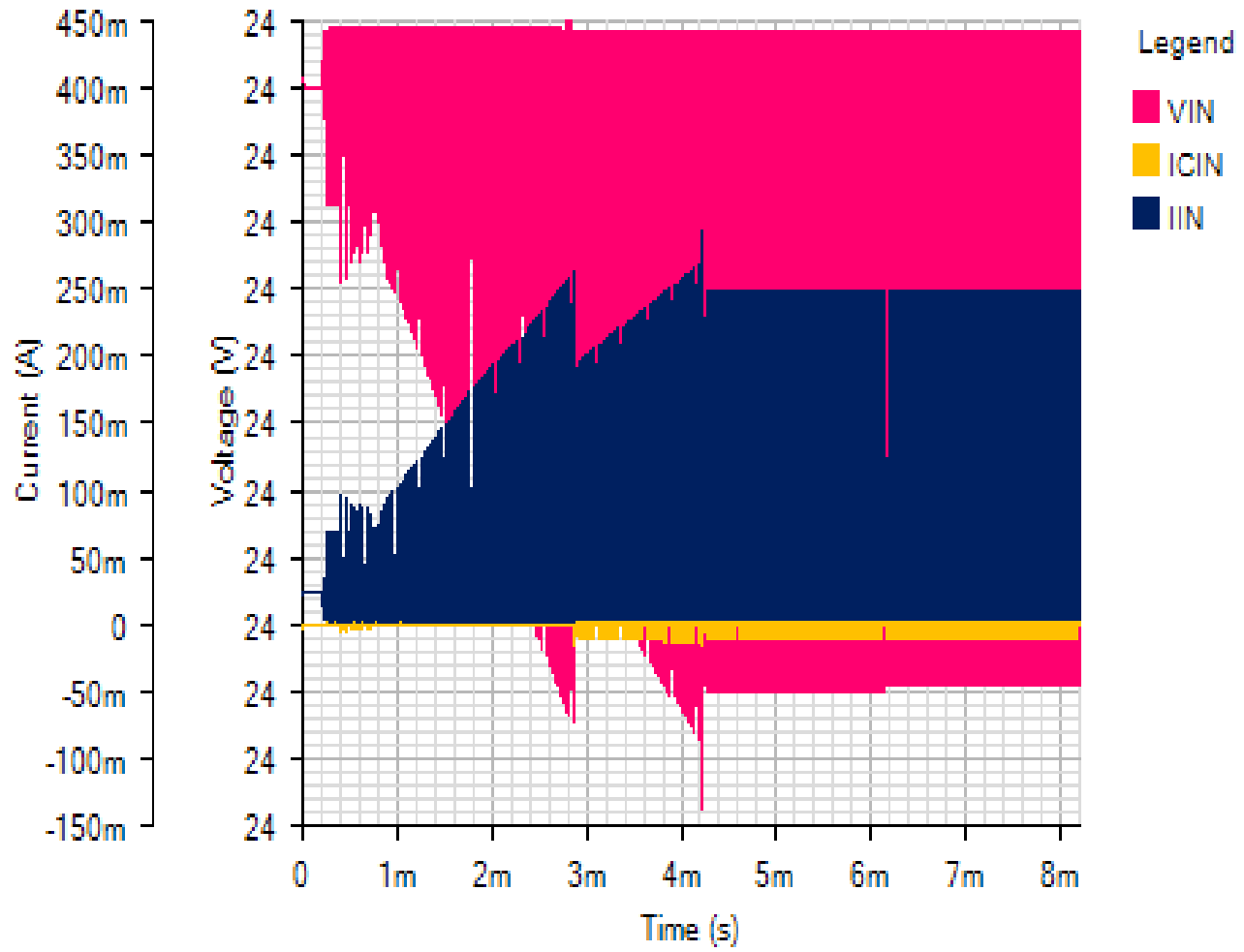


Start Up - Mon Jan 07 2019 10:28:36



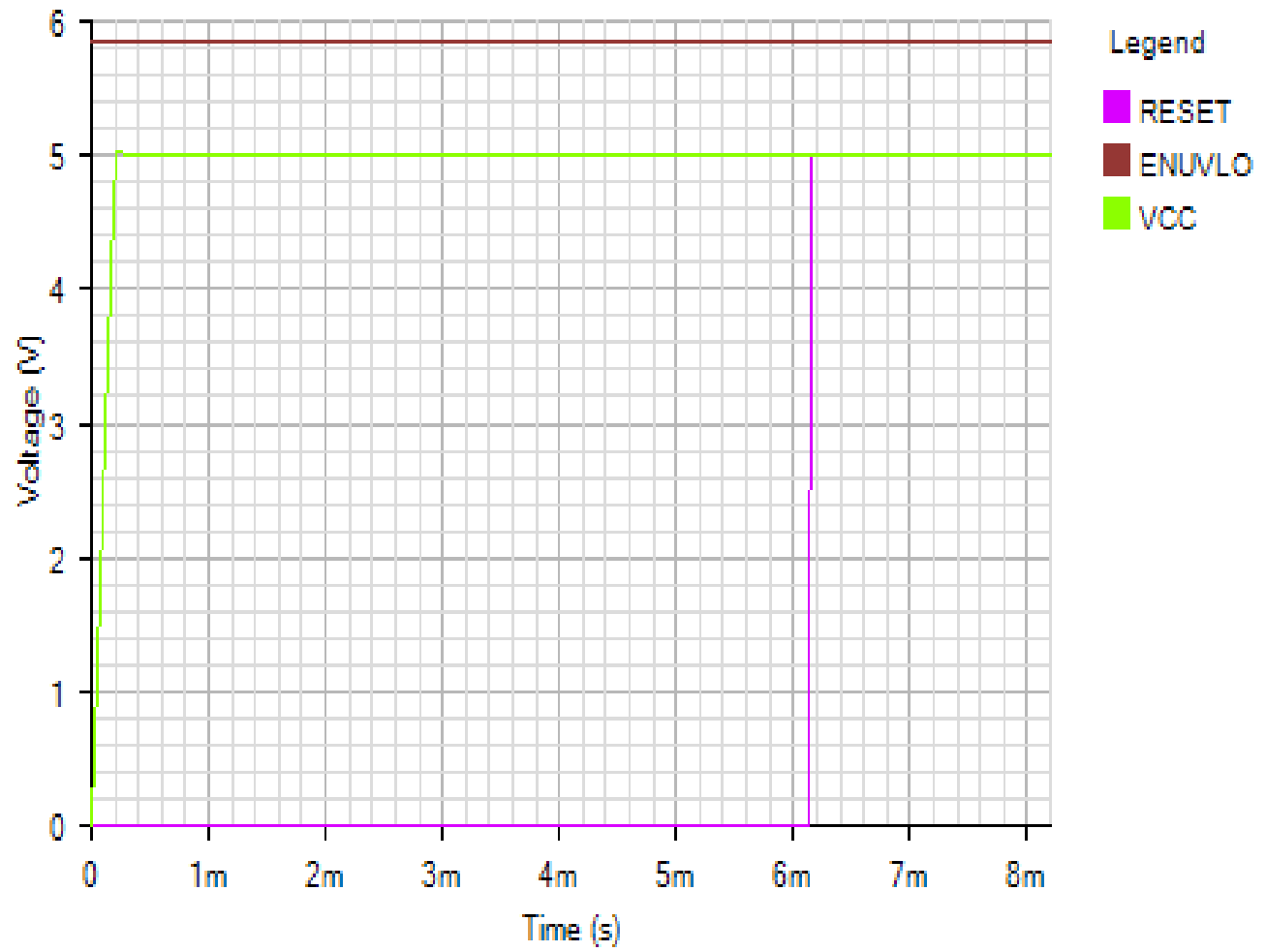
INPUT

Default



IC

Default



OUTPUT

Default

