

Initial Design

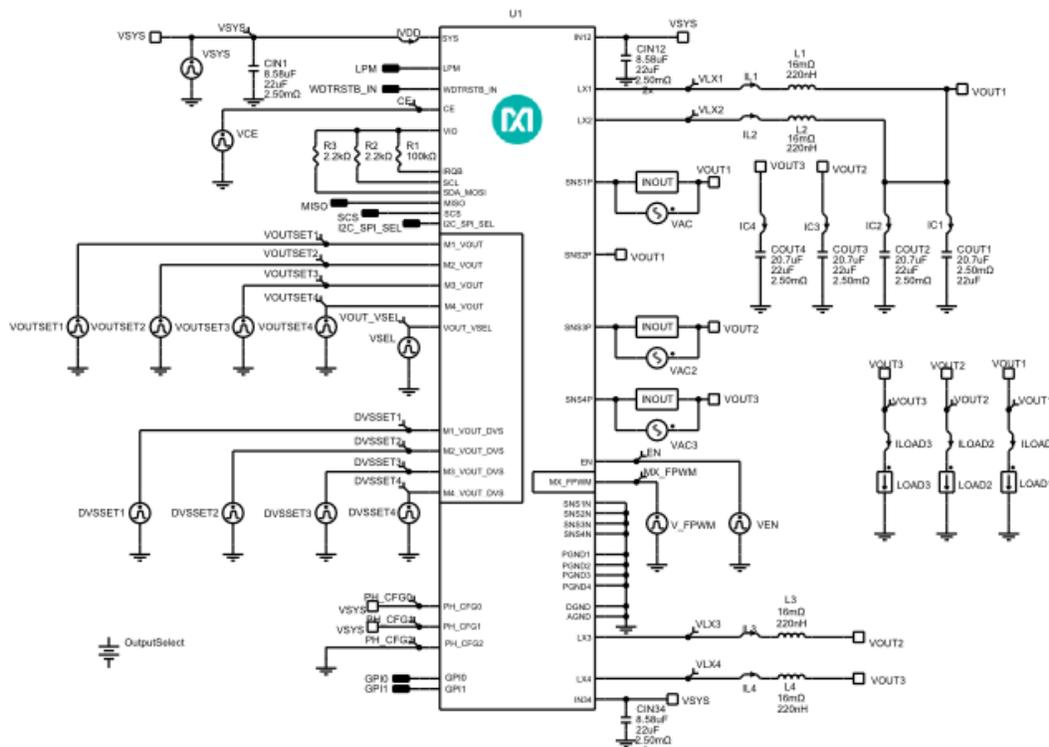
1.0

Design Requirements

Parameter	Value
Phase Configuration	2 1 1 Phase
Min. Input Voltage	3.3V
Max. Input Voltage	4.2V
Typ. Input Voltage	3.6V
Output Voltage 1	0.65V
DVS Output 1	1V
Output Current 1	5A
Output Voltage 2	0.65V
DVS Output 2	1V
Output Current 2	5A
Output Voltage 3	0.65V
Output Current 3	5A
DVS Output 3	1V
Output Voltage 4	0V
DVS Output 4	0V
Output Current 4	5A
Performance Priority	Balance Efficiency and Size
BOM Priority	Cost
Mode of Operation	Forced PWM
Output Active Discharge Enable	0 = 100Ω discharge resistance is disabled when EN is low.
Soft Start Slew Rate Selection	110b = Sets slew rate to 60mV/μs
Shut Down Slew Rate Selection	110b = Sets slew rate to 60mV/μs
Ramp-Up Slew Rate Selection	110b = Sets slew rate to 60mV/μs

Parameter	Value
Ramp-Down Slew Rate Selection	110b = Sets slew rate to 60mV/μs
PMOS Peak/NMOS Valley Current Limit	101b: 6.0A / 4.0A
Output 2 Start Up Delay	0S
Output 3 Start Up Delay	0S
Output 4 Start Up Delay	0S
Output 1 Shut Down Delay	0S
Output 2 Shut Down Delay	0S
Output 3 Shut Down Delay	0S
Output 4 Shut Down Delay	0S

Schematic



Simulation Note (For Online Only)

Only one output can be active when a POP (Periodic Operating Point) Analysis is selected since a periodic operating point cannot be found for multiple outputs operating at independent frequencies. Only one output will be simulated at a time for Load Stop, Steady State, AC Loop, Line Transient, Output Voltage Change, and Efficiency simulations.

To select which output is simulated, change the OutputSelect voltage in each simulation window to match the output voltage (1 for Vout1, 2 for Vout2, 3 for Vout3, 4 for Vout4). Only the selected output will be simulated with the other outputs disabled and the displayed waveforms will show only the active output waveforms as operational. Start Up and Shut Down are simulated with all outputs active and waveforms are displayed with all outputs active.

NOTES

Mx_VOUT, Mx_VOUT_DVS, VOUT_VSEL are fictitious pins. They are used to simulate writing to the VOUT_D and VOUT_S registers dynamically with an analog voltage source.

Mx_FPWM is a fictitious pin. This is used to simulate writing to the Mx_FPWM register with a digital voltage source.

VI0, IRCB, SCL, SDA_MOSI, MISO, SCS, I2C_SPL_SEL, and WDSTRSTB_IN are not functional pins and are there only for completeness.

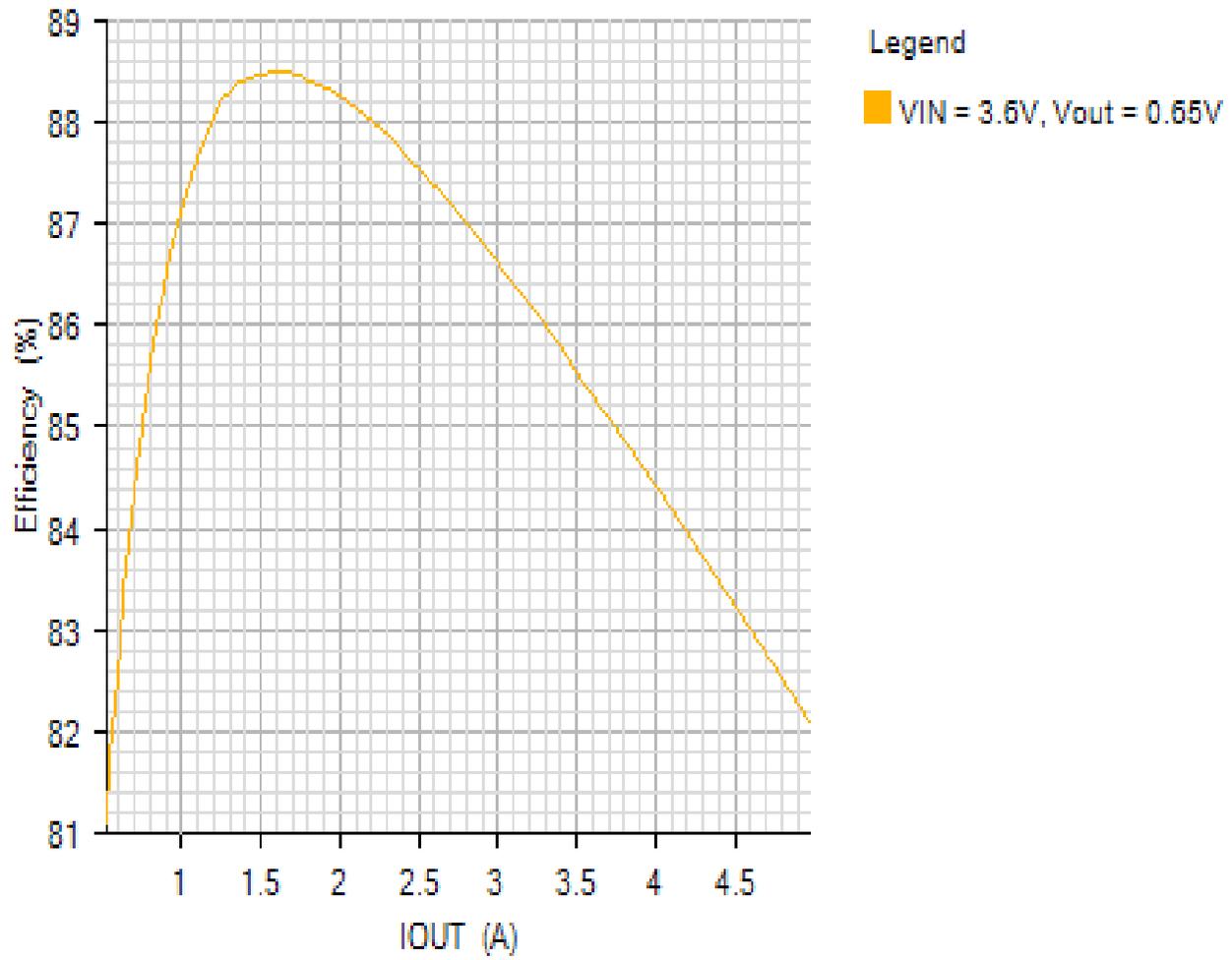
BOM

Ref	Qty	Part Number	Manufacturer	Description
U1	1	MAX77812	User-Defined	IC
CIN1	1	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
CIN12	2	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
CIN34	2	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
COUT1	1	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
COUT2	1	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
COUT3	1	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
COUT4	1	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
L1	1	HMLE20161B-R22MDR	Cyntec	Inductor 220nH 13mOhm 5.8A Isat 5.3A Irms
L2	1	HMLE20161B-R22MDR	Cyntec	Inductor 220nH 13mOhm 5.8A Isat 5.3A Irms
L3	1	HMLE20161B-R22MDR	Cyntec	Inductor 220nH 13mOhm 5.8A Isat 5.3A Irms
L4	1	HMLE20161B-R22MDR	Cyntec	Inductor 220nH 13mOhm 5.8A Isat 5.3A Irms
R1	1	CRG0603-Q-104JT	Venkel	Res Thick Film 0603 100K Ohm 5% 0.1W(1/10W) ±200ppm/°C Pad SMD T/R
R2	1	RC0603JR-072K2P	Yageo	Res Thick Film 0603 2.2K Ohm 5% 0.1W(1/10W) ±150ppm/°C Epoxy Pad SMD T/R
R3	1	RC0603JR-072K2P	Yageo	Res Thick Film 0603 2.2K Ohm 5% 0.1W(1/10W) ±150ppm/°C Epoxy Pad SMD T/R

Simulation Results
Efficiency - Mon Nov 19 2018 17:59:28

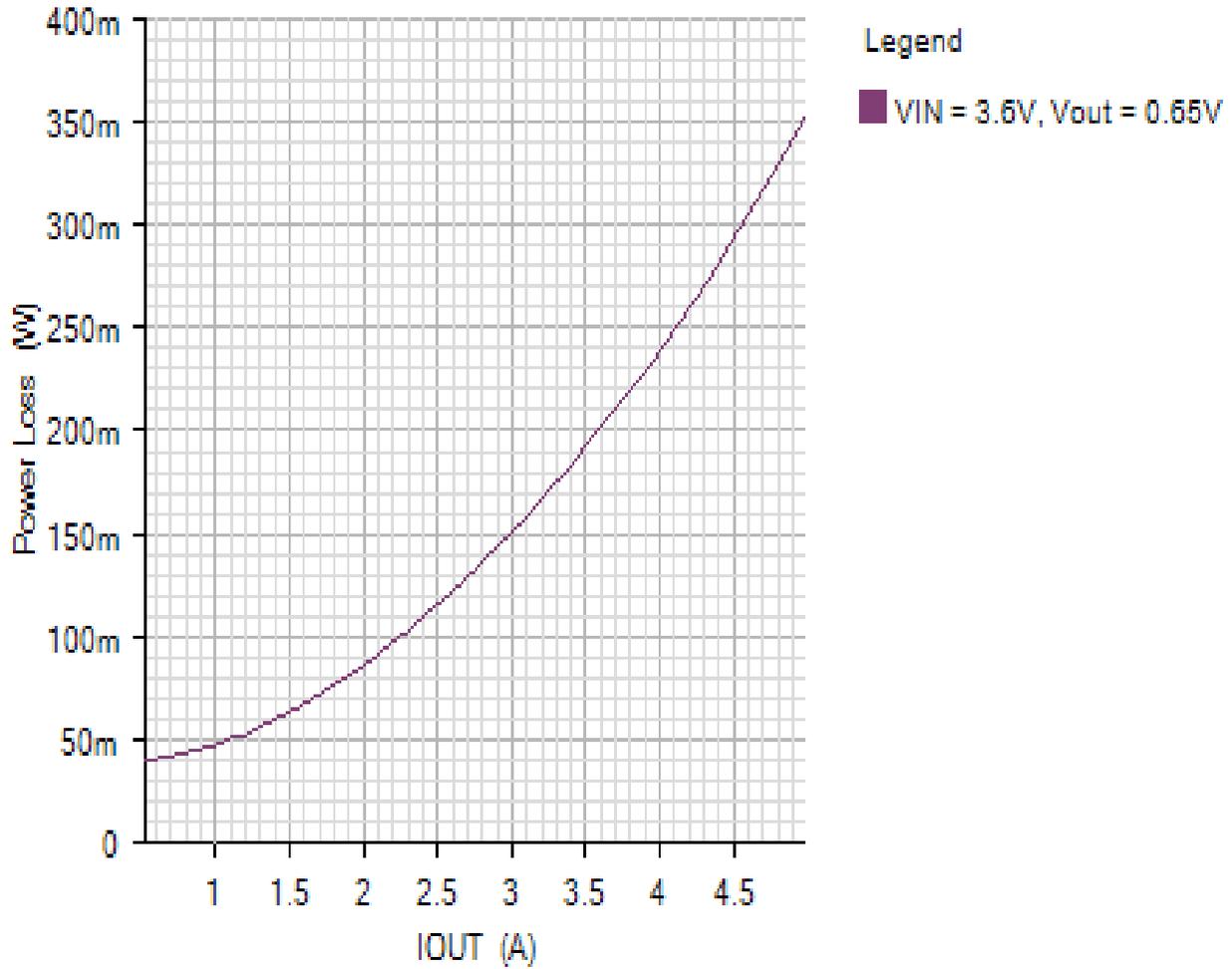
EFFICIENCY_PLOT

Default

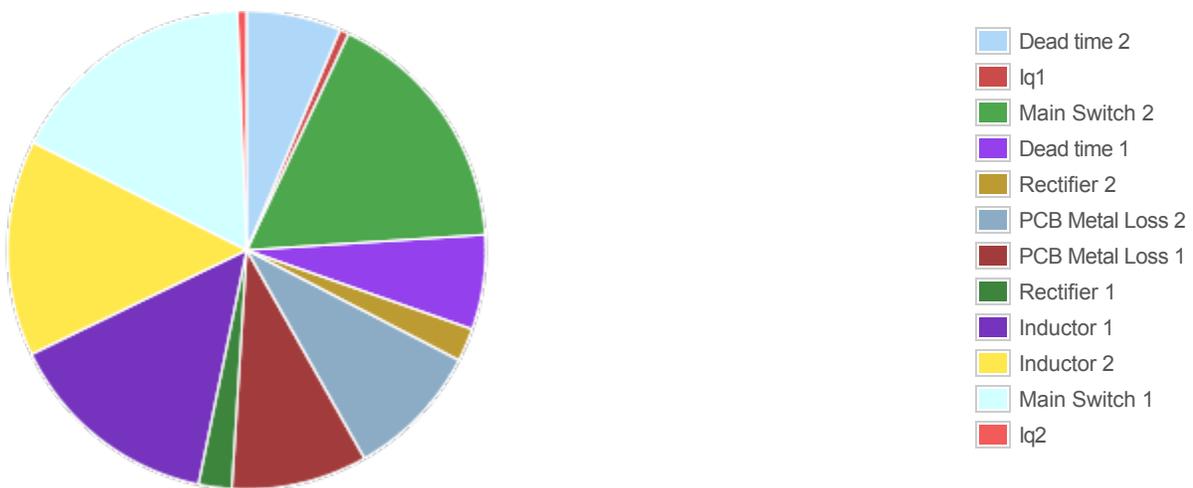


POWER_LOSS_PLOT

Default



Losses



Component

Loss (W)

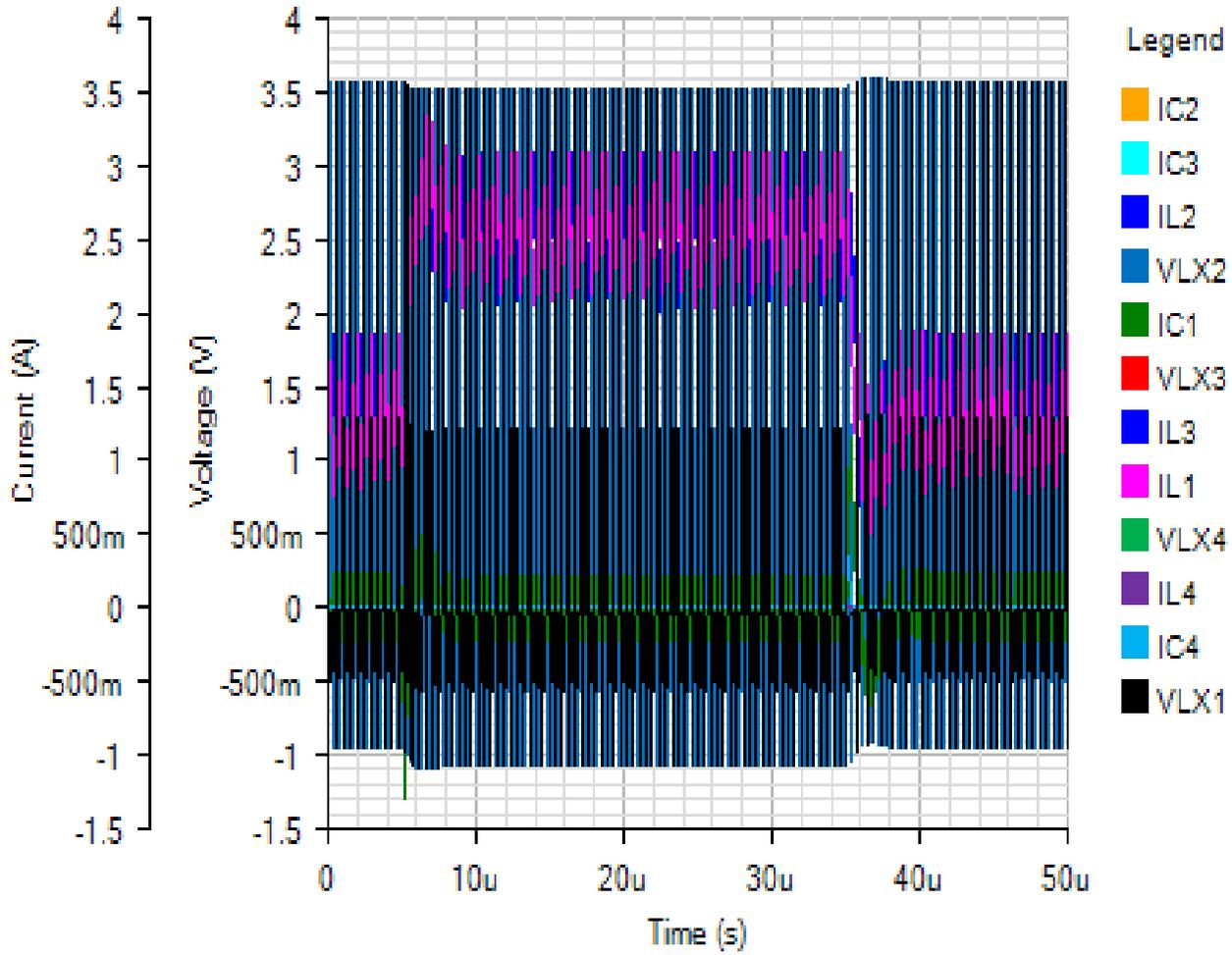
% of total

Component	Loss (W)	% of total
Dead time 2	0.166184	6.4
Iq1	0.0162	0.6
Main Switch 2	0.440898	17
Dead time 1	0.166184	6.4
Rectifier 2	0.058436	2.2
PCB Metal Loss 2	0.239058	9.2
PCB Metal Loss 1	0.239058	9.2
Rectifier 1	0.058436	2.2
Inductor 1	0.37942	14.6
Inductor 2	0.37942	14.6
Main Switch 1	0.440898	17
Iq2	0.0162	0.6
Total	2.600392	100

Load Step - Mon Nov 19 2018 17:59:28

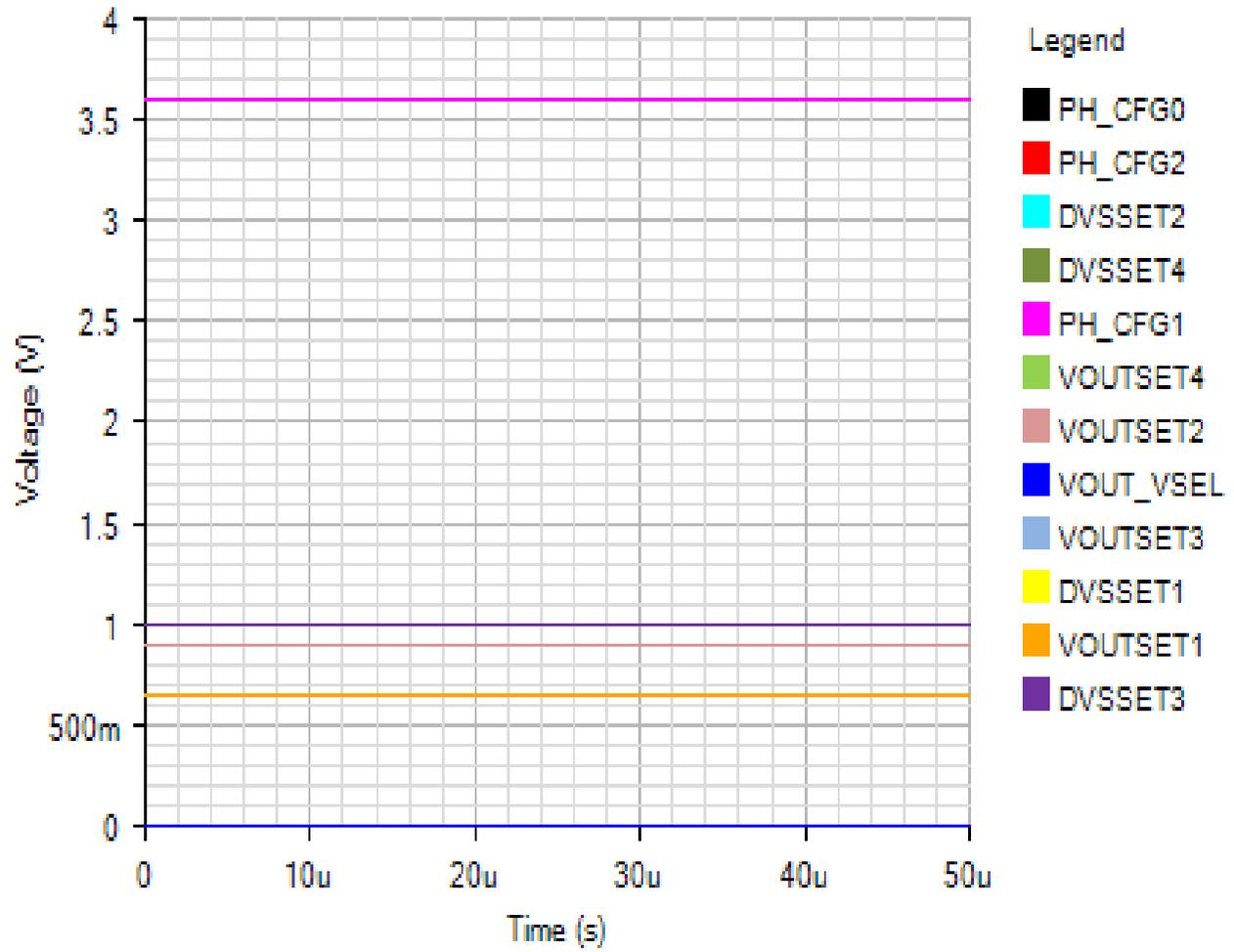
SWITCHING

Default



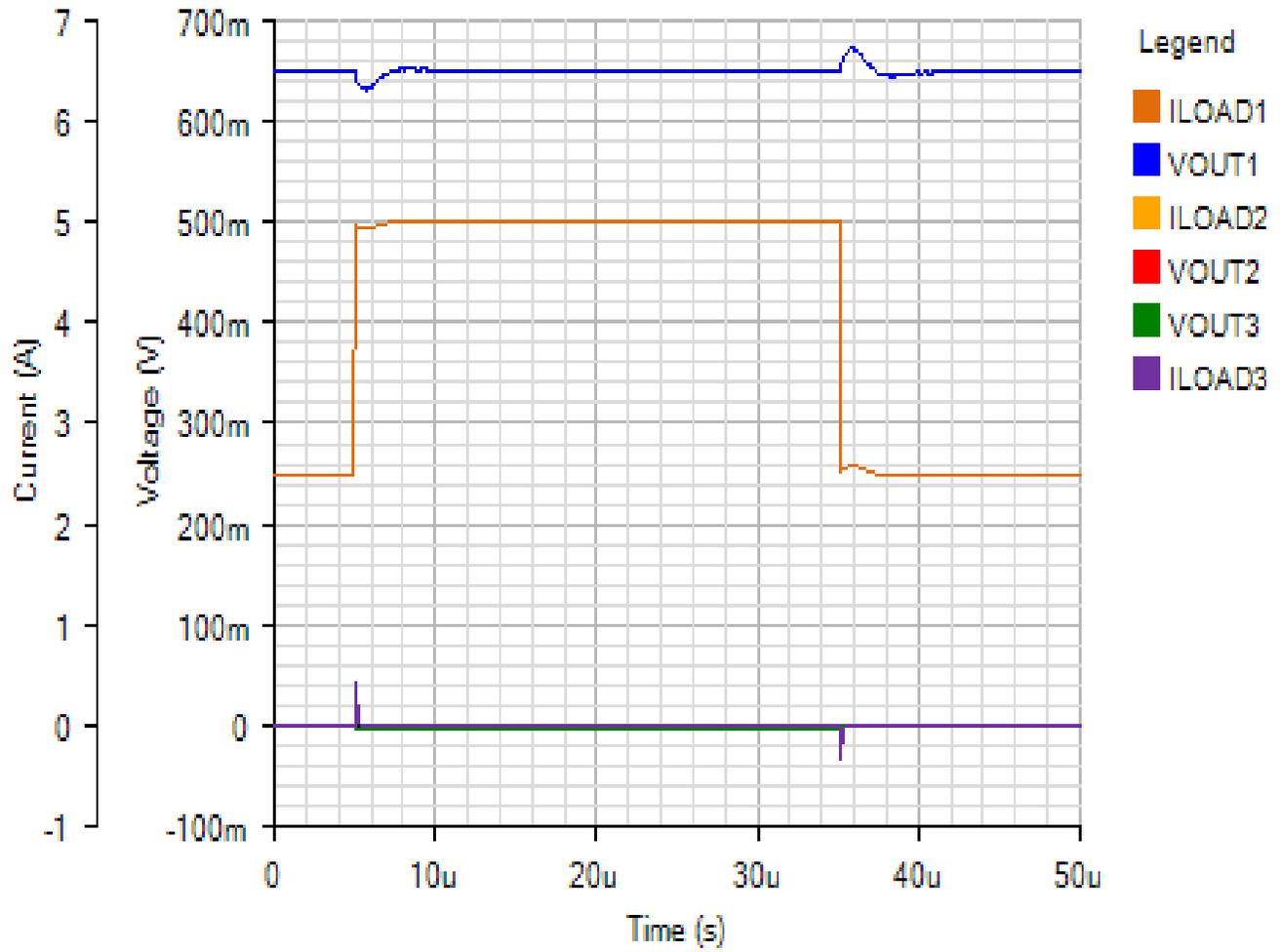
IC

Default



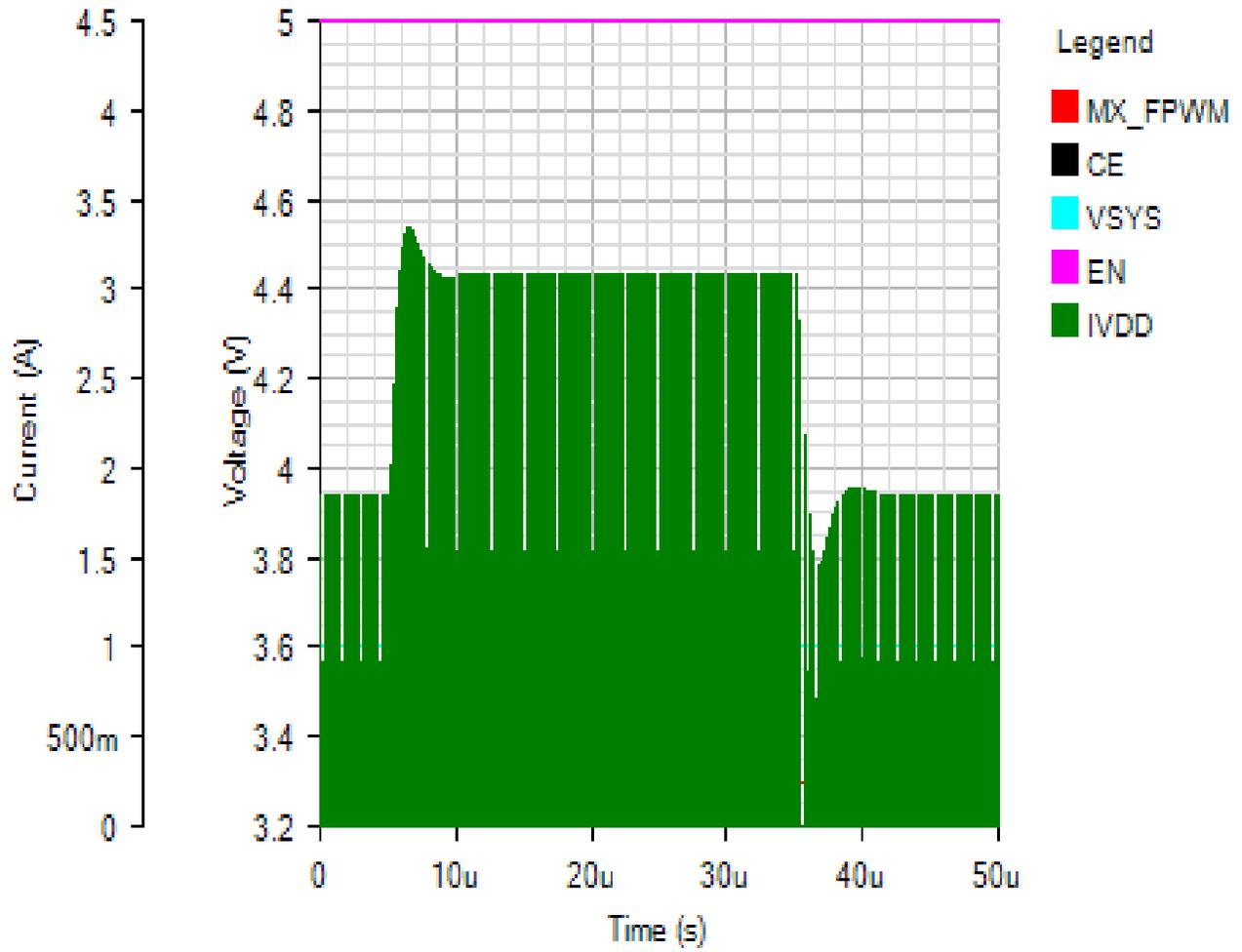
OUTPUT

Default

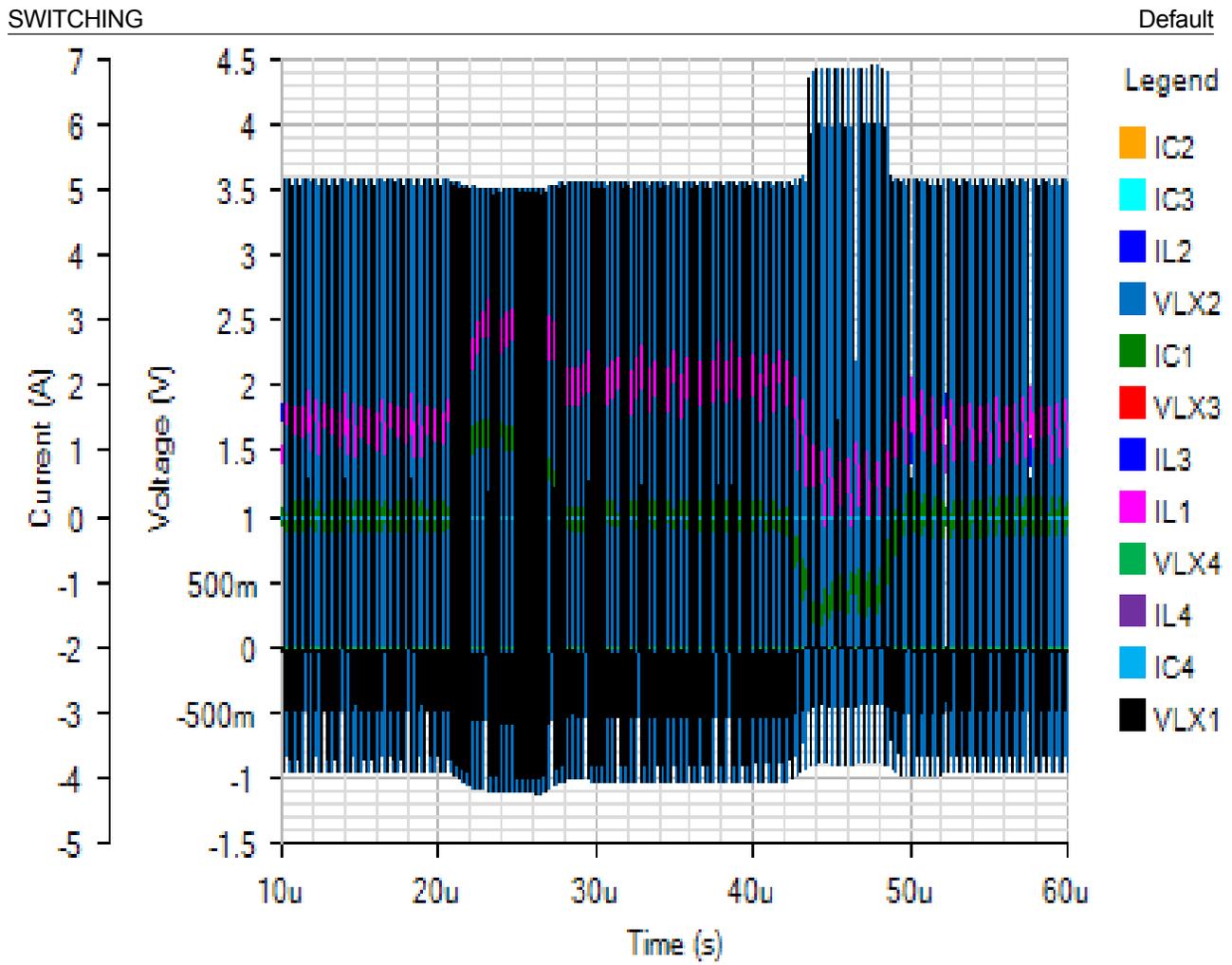


INPUT

Default

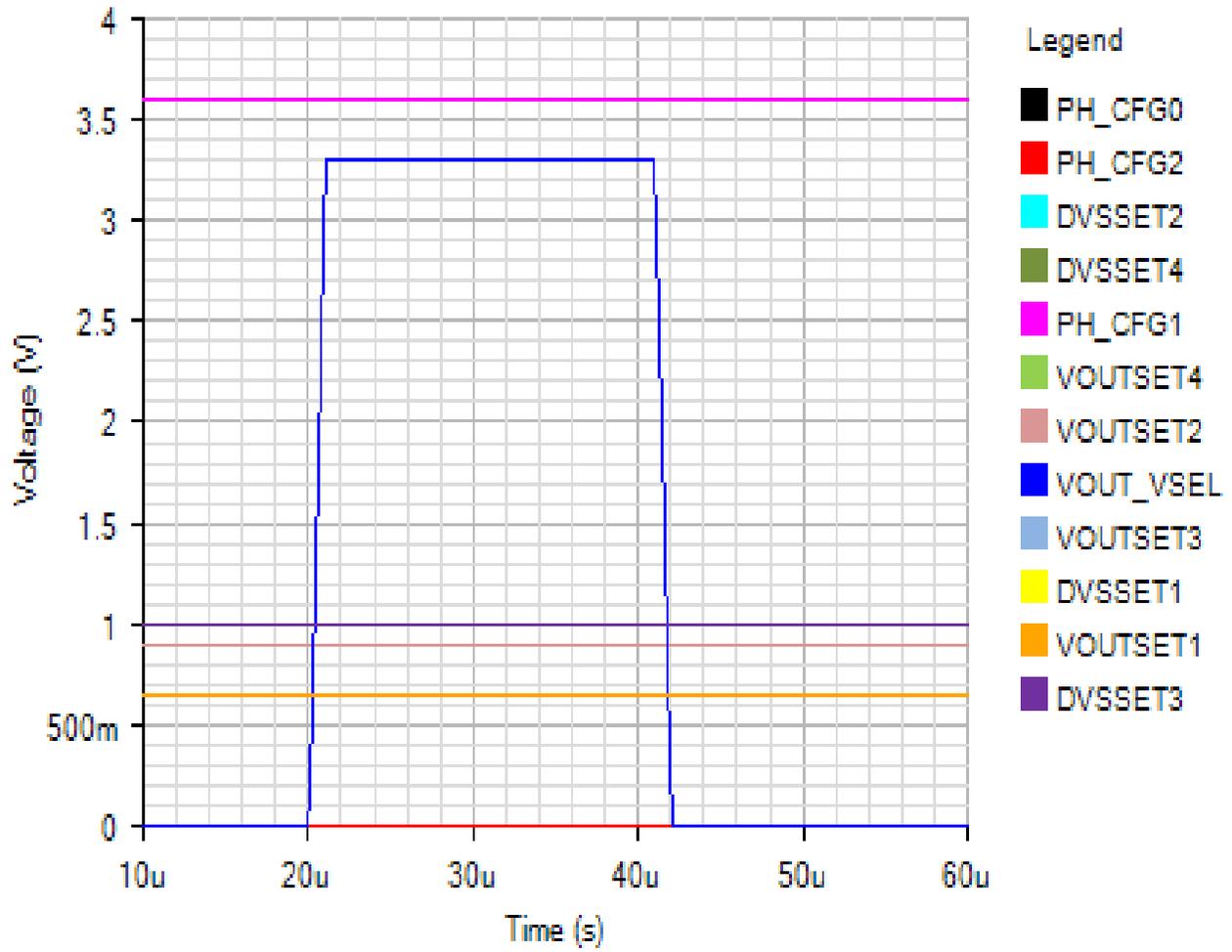


Output Voltage Change - Mon Nov 19 2018 17:59:28



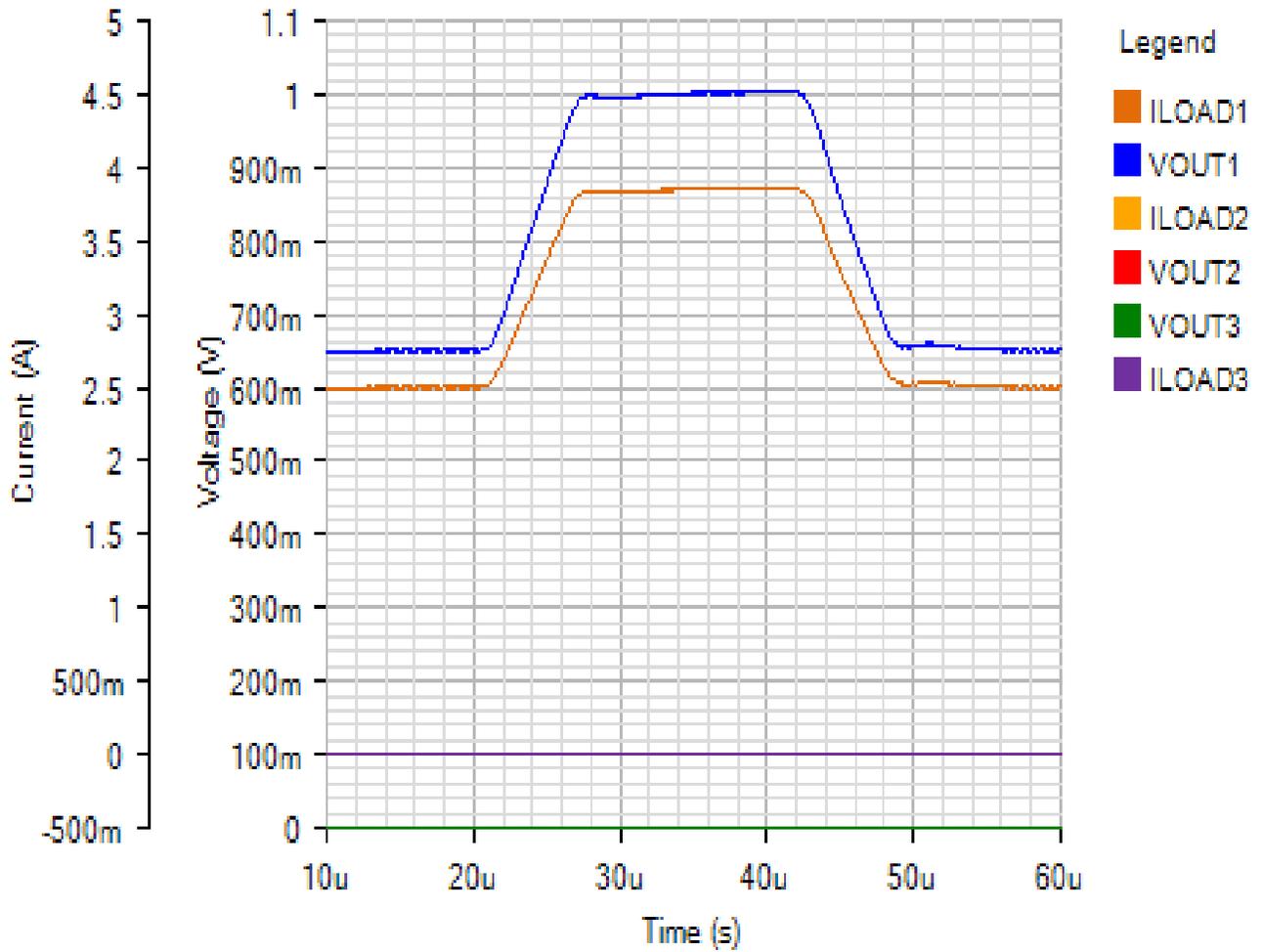
IC

Default



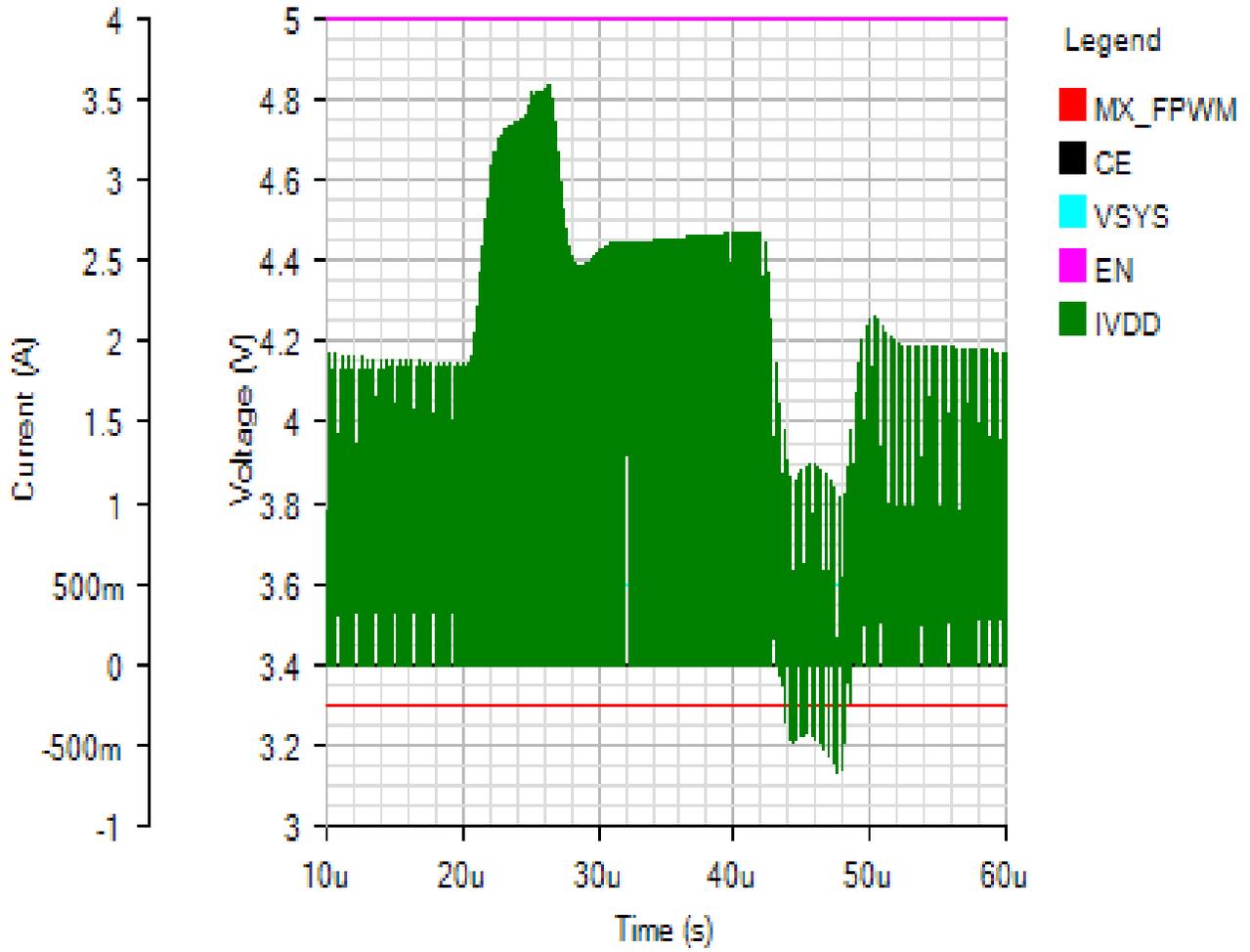
OUTPUT

Default



INPUT

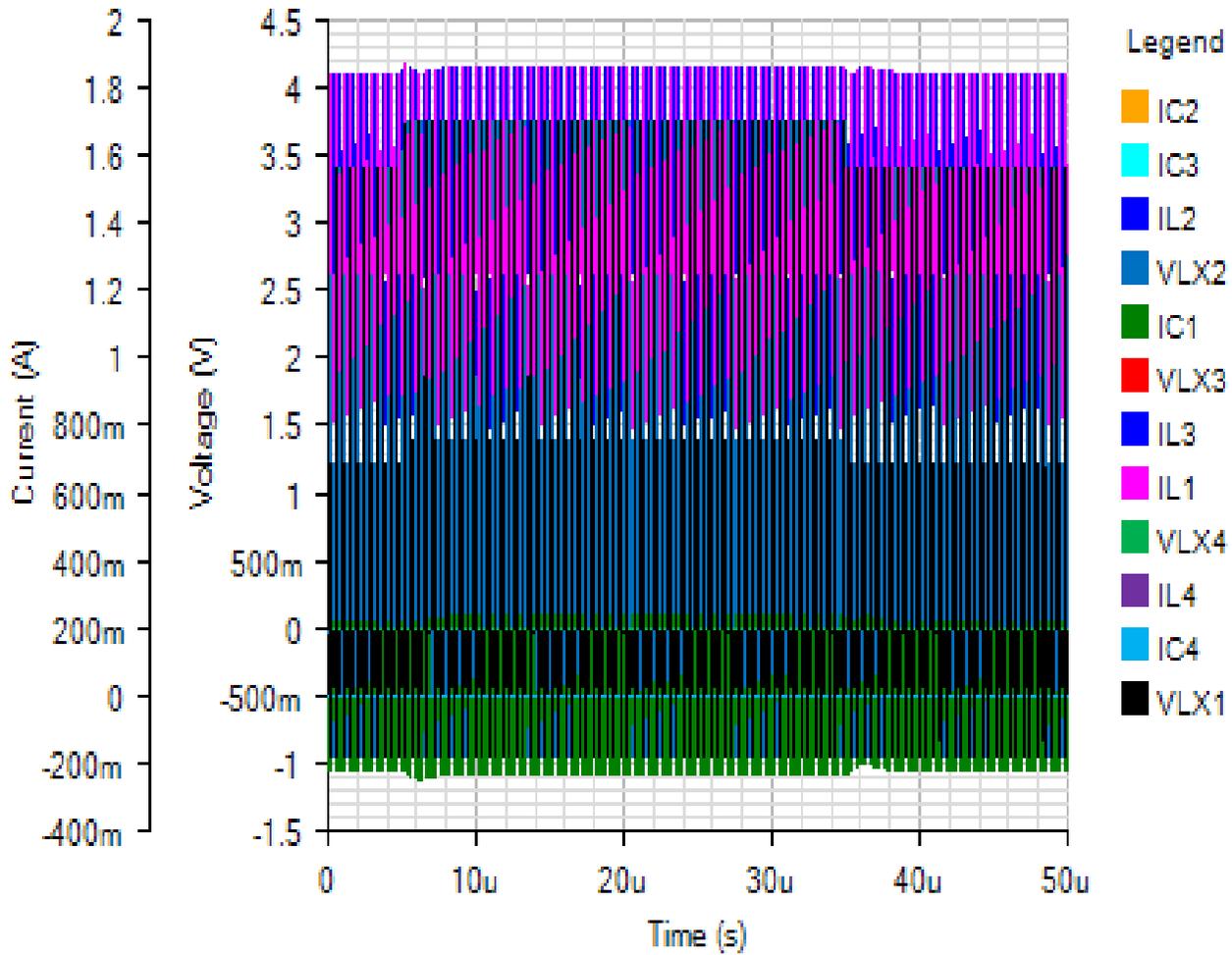
Default



Line Transient - Mon Nov 19 2018 17:59:28

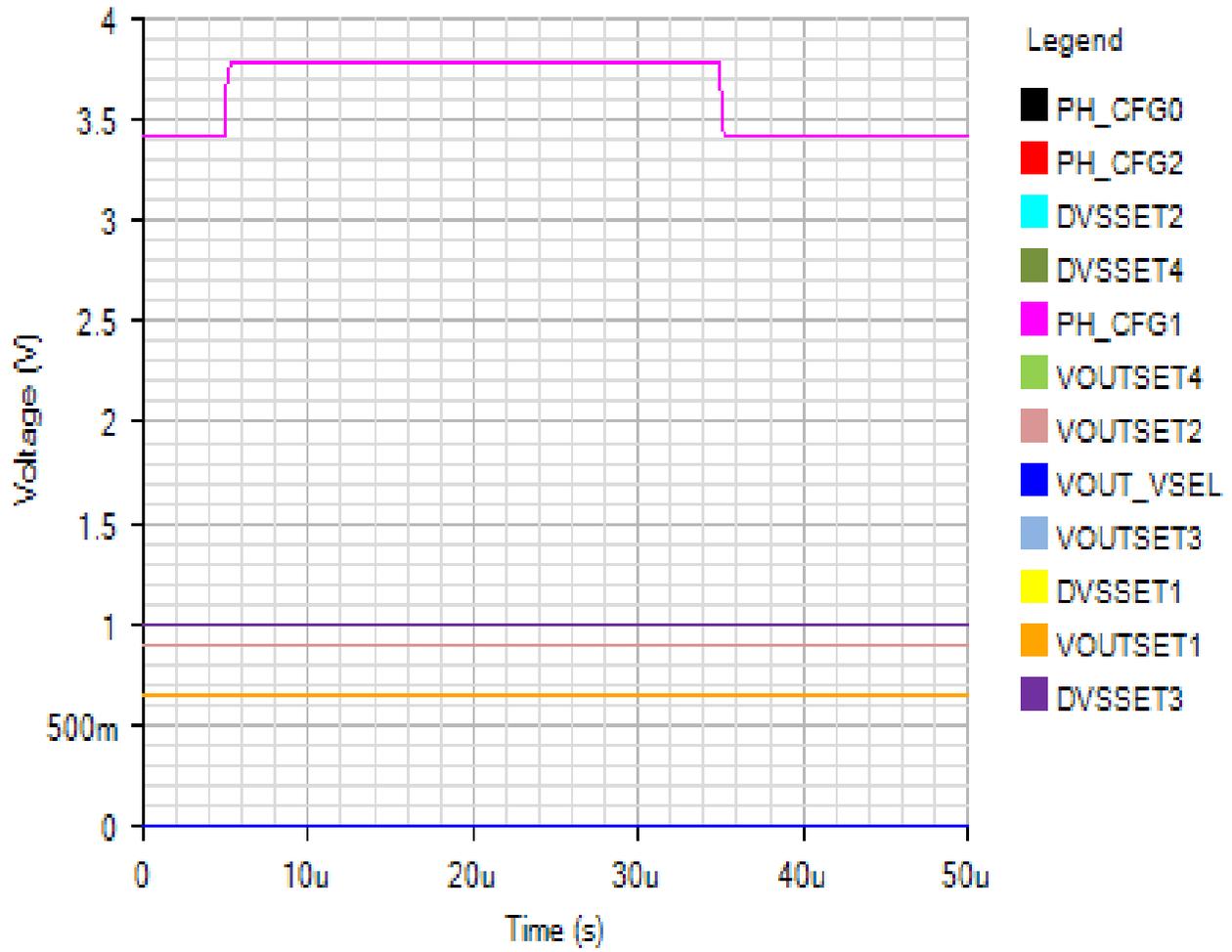
SWITCHING

Default



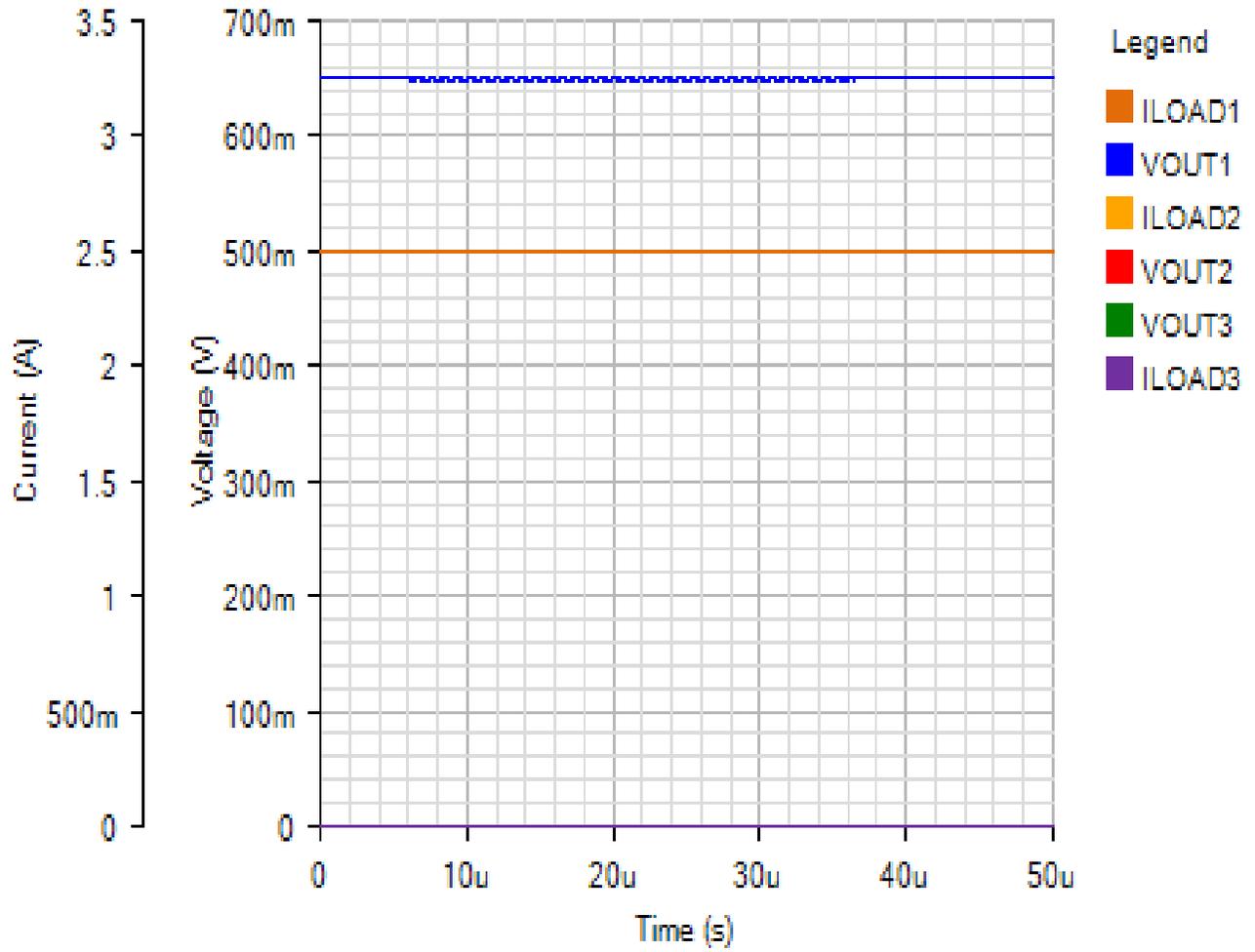
IC

Default



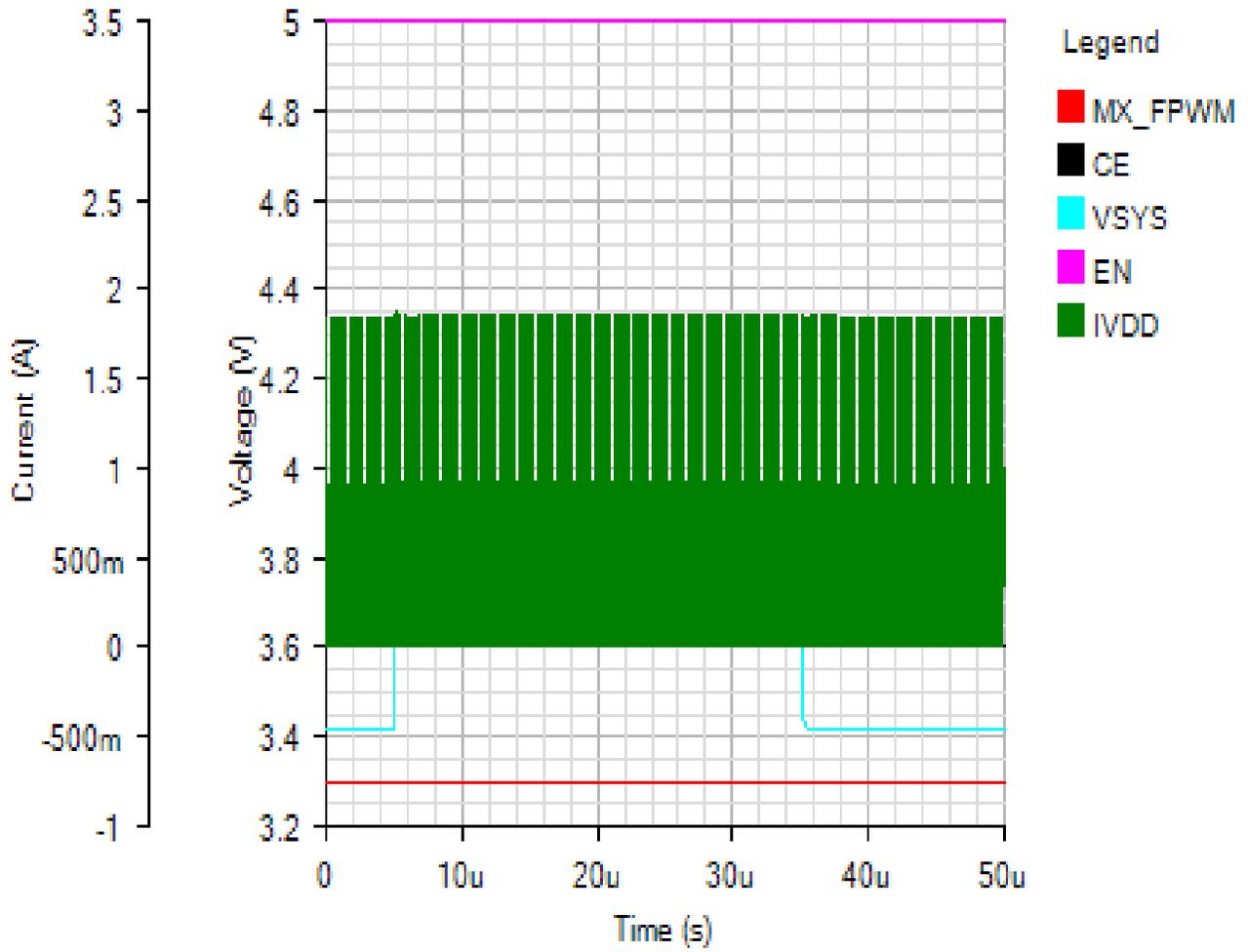
OUTPUT

Default



INPUT

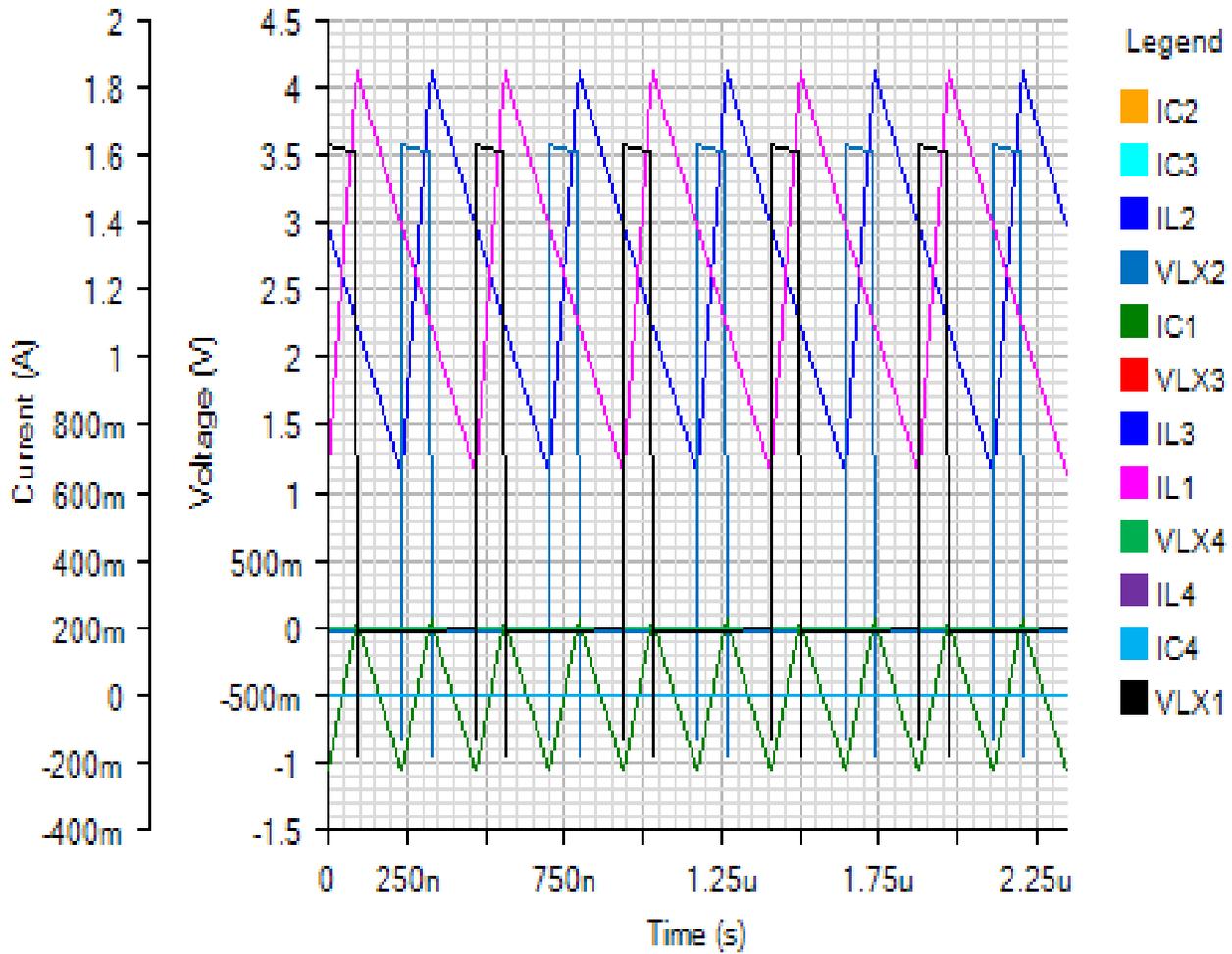
Default



Steady State - Mon Nov 19 2018 17:59:28

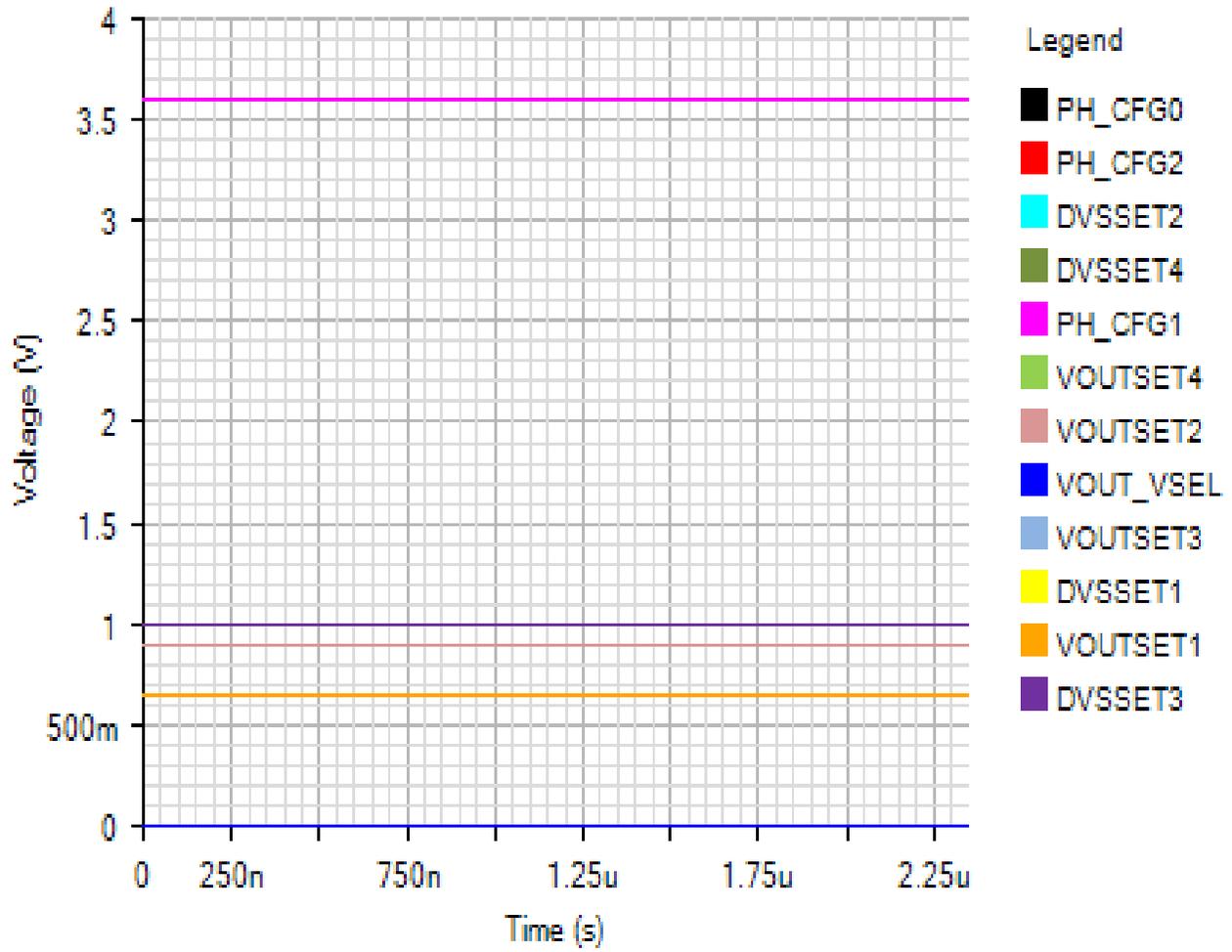
SWITCHING

Default



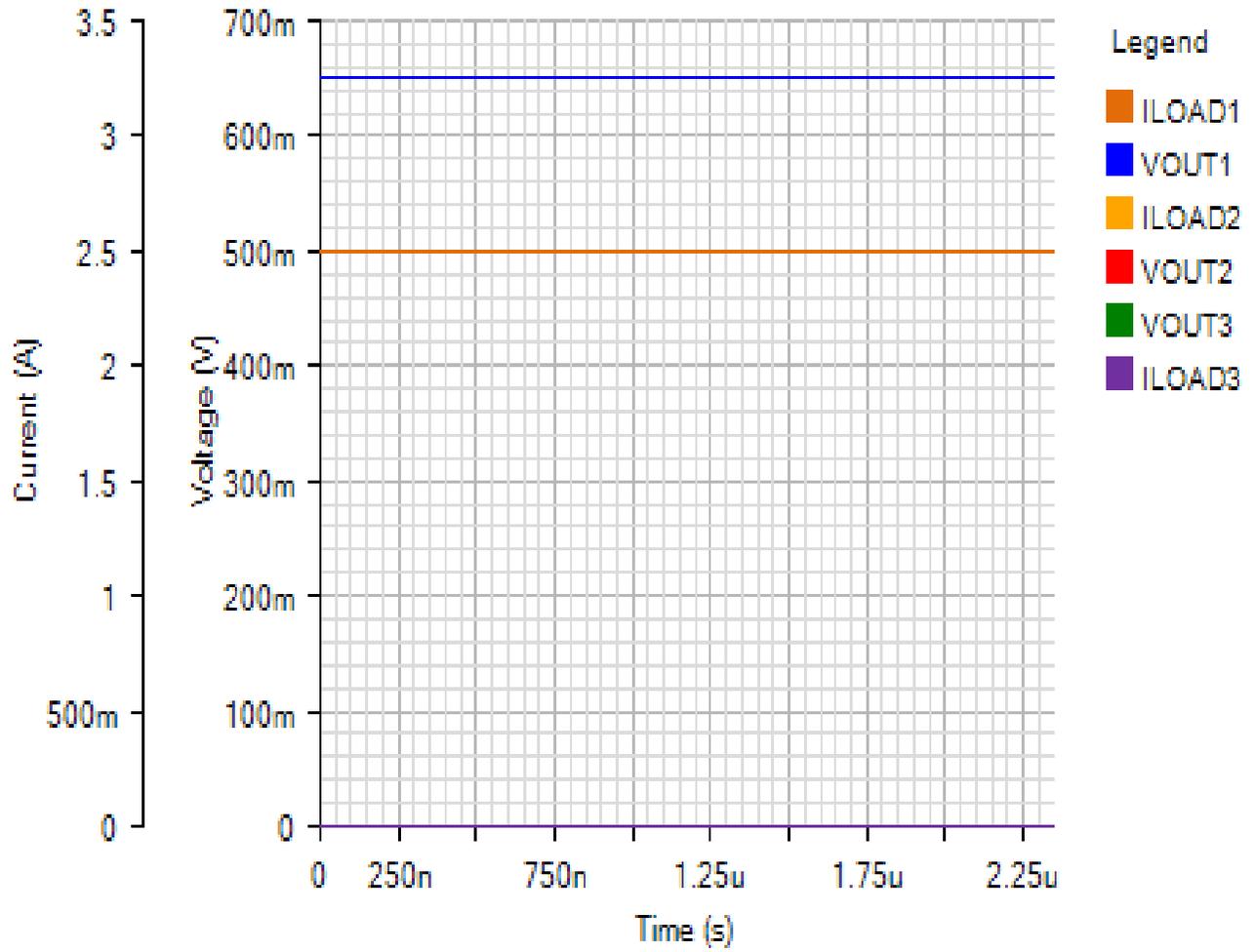
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Default



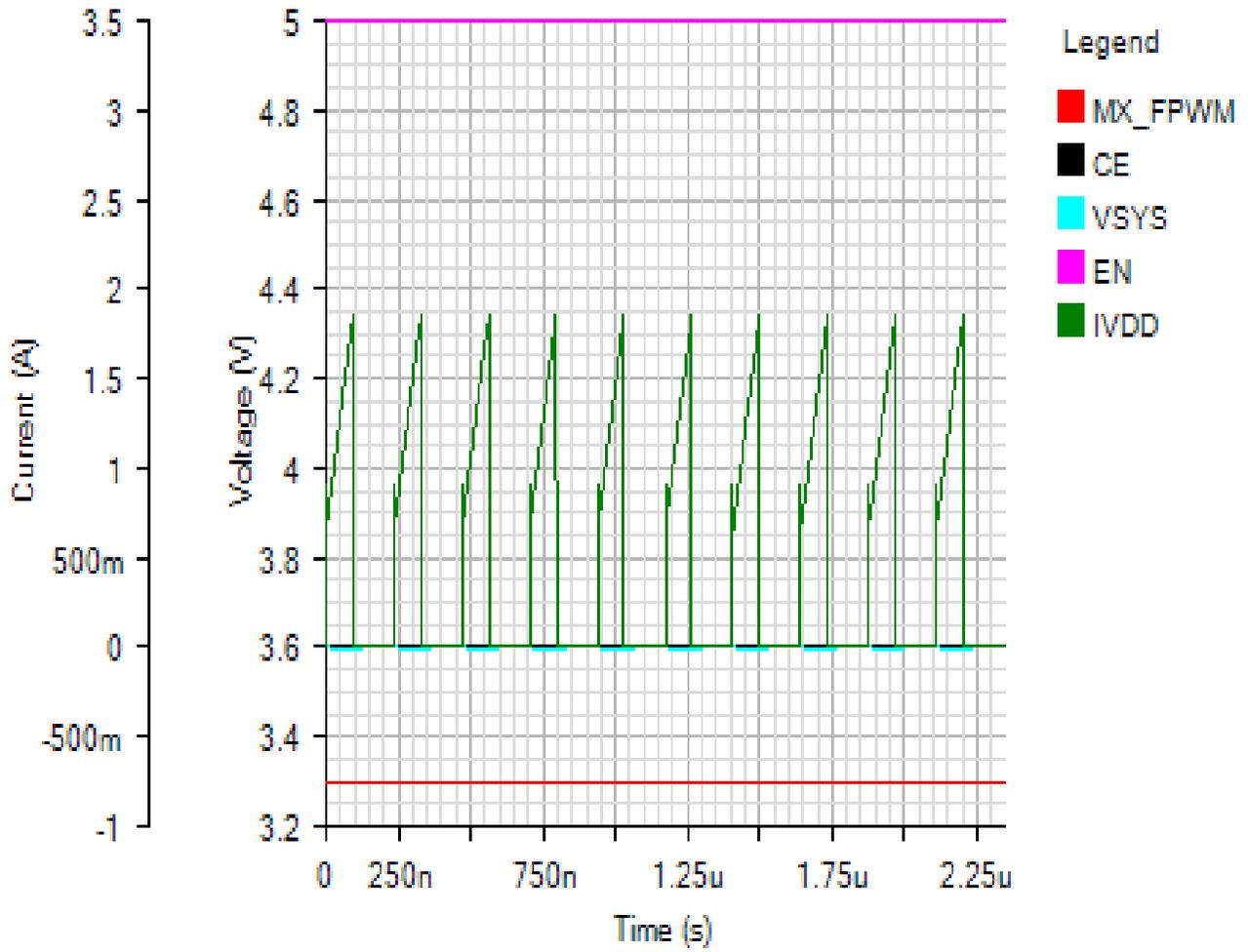
OUTPUT

Default



INPUT

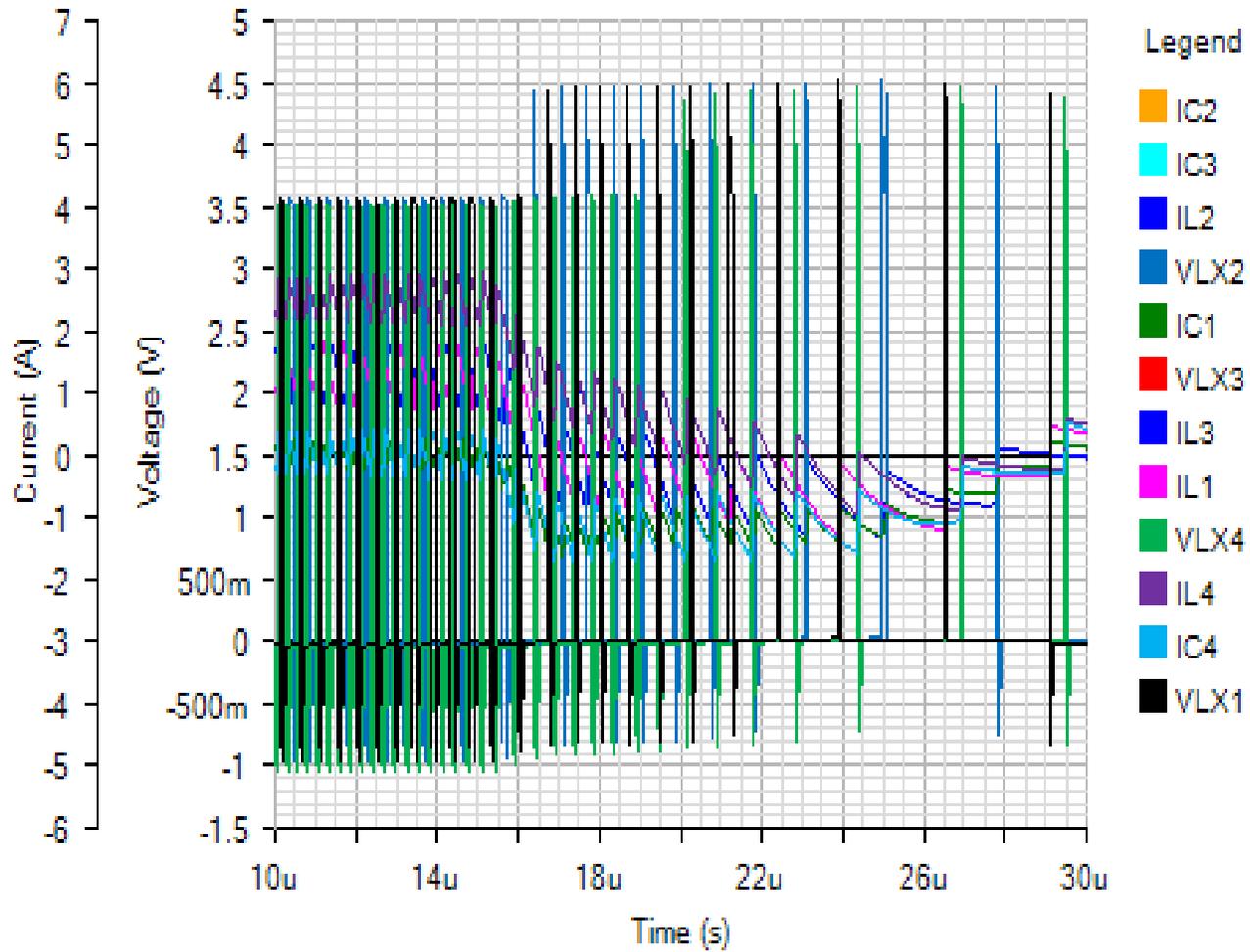
Default



Shut Down - Mon Nov 19 2018 17:59:28

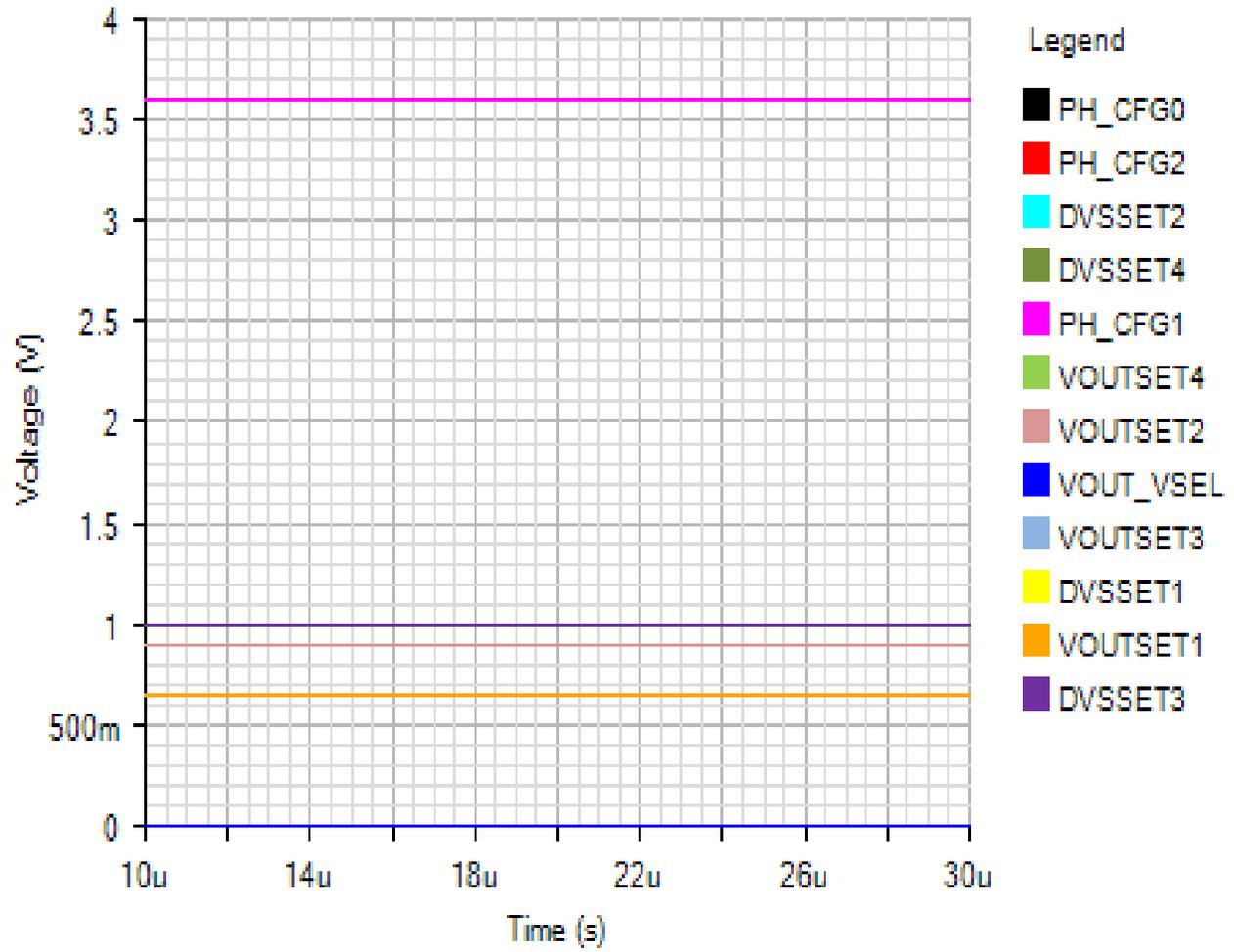
SWITCHING

Default



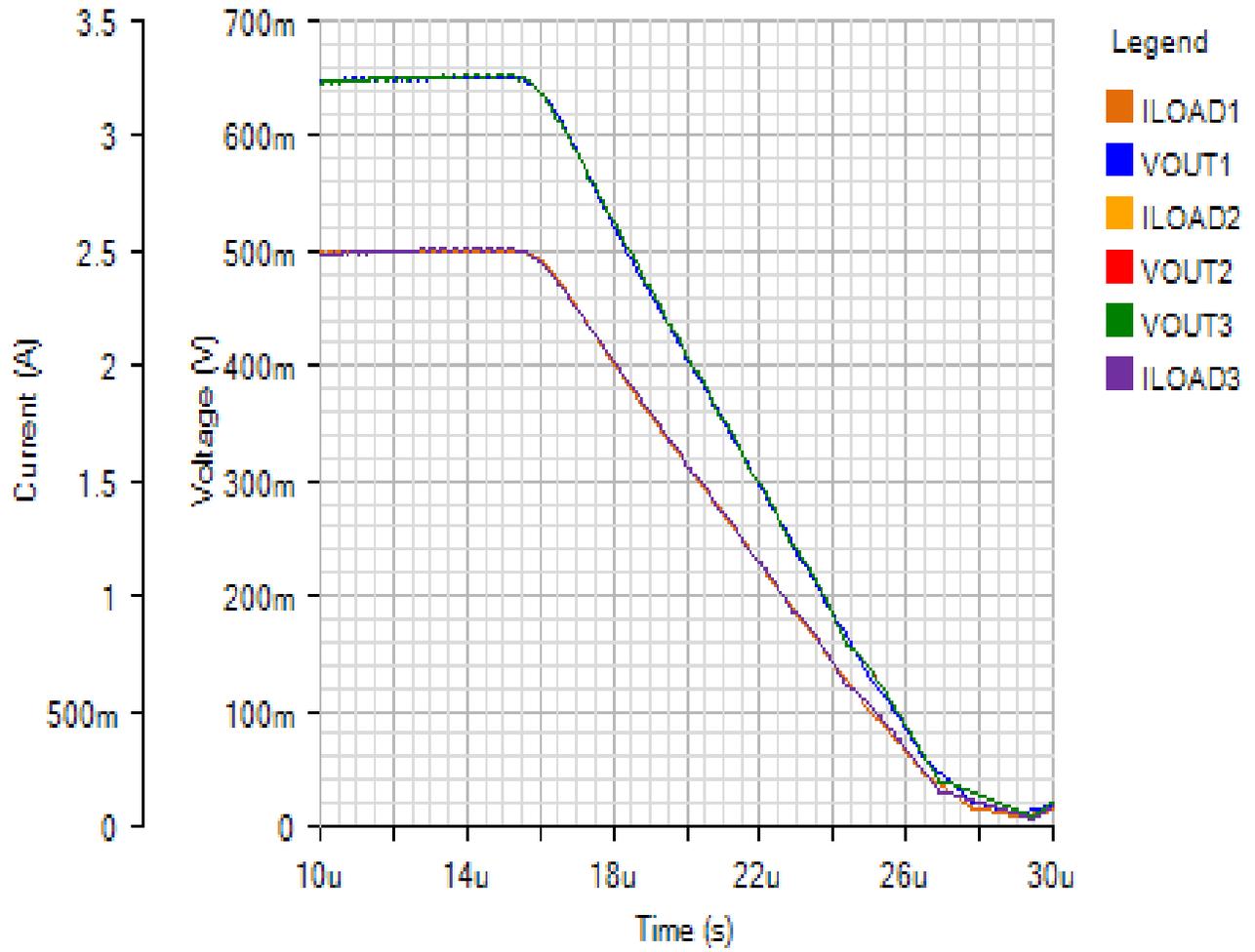
IC

Default



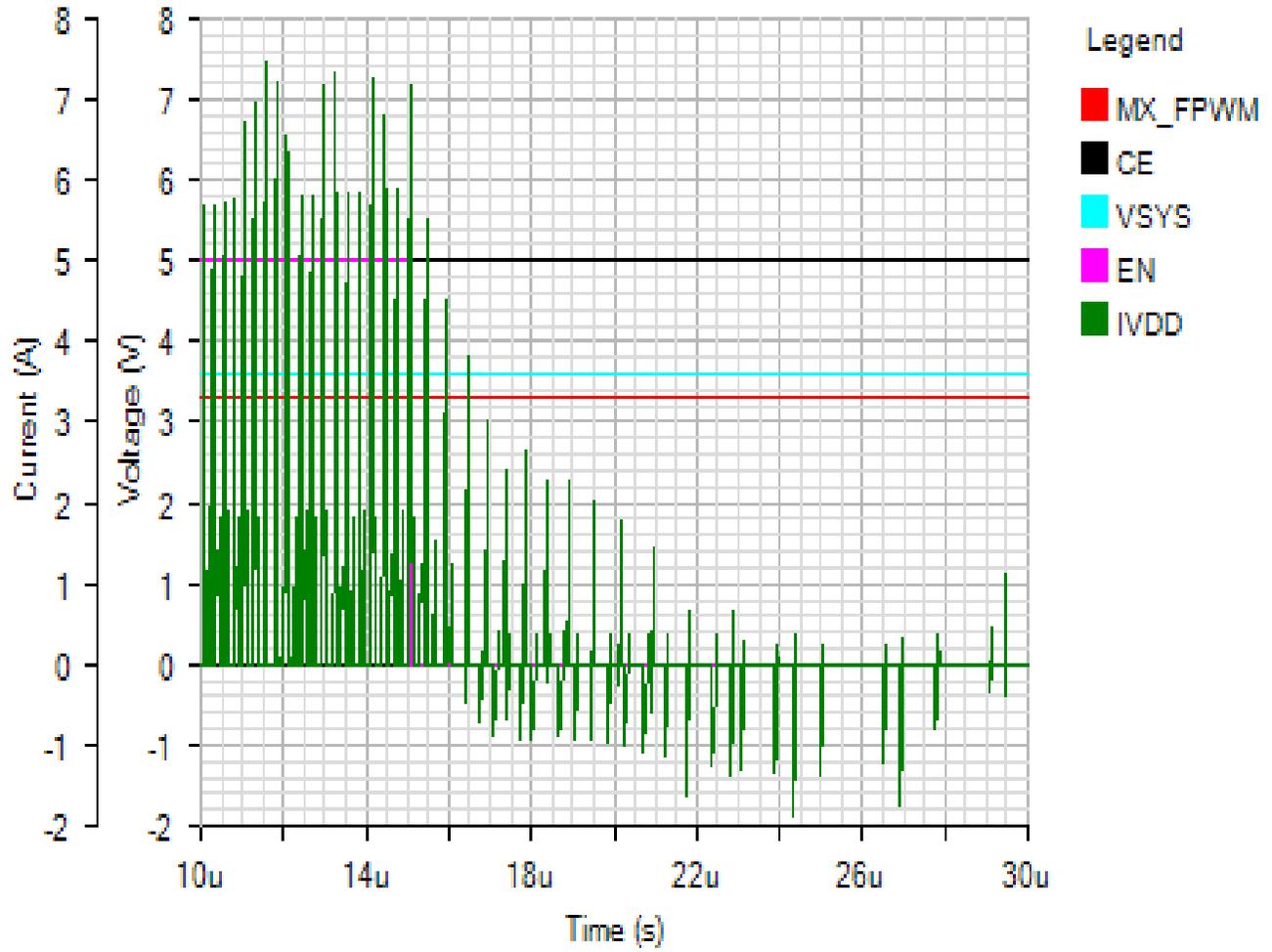
OUTPUT

Default



INPUT

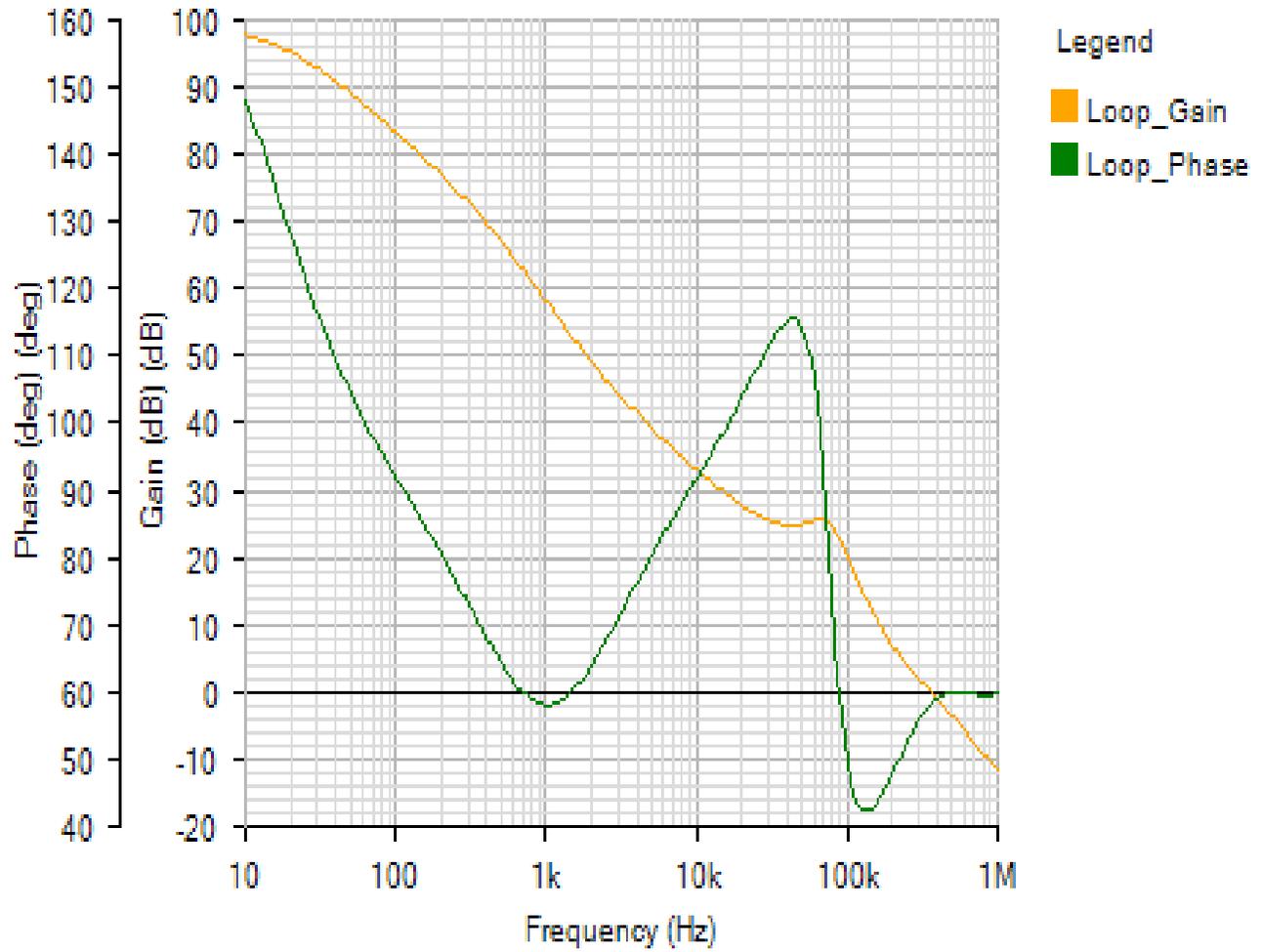
Default



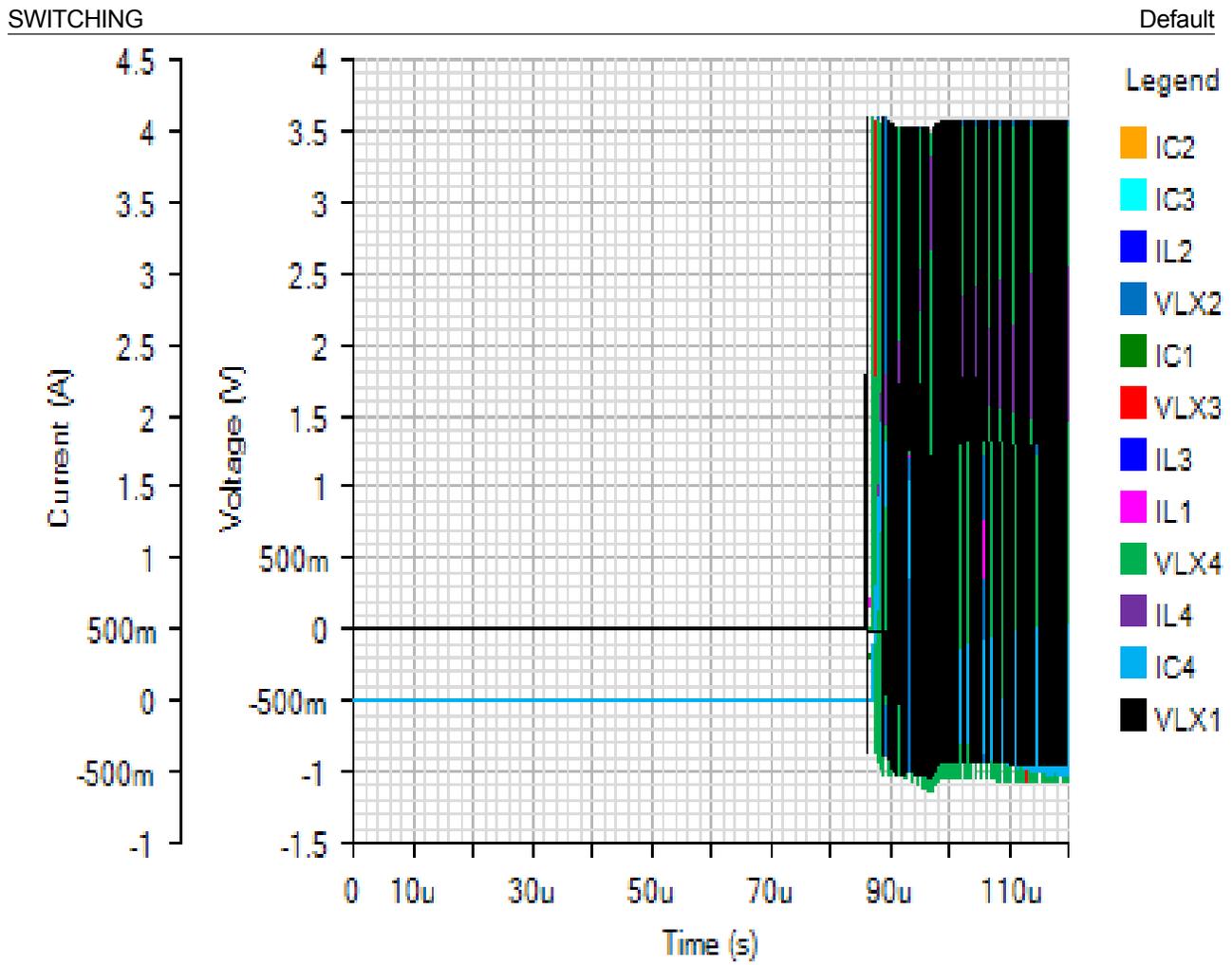
AC Loop - Mon Nov 19 2018 17:59:28

BODE1

Default

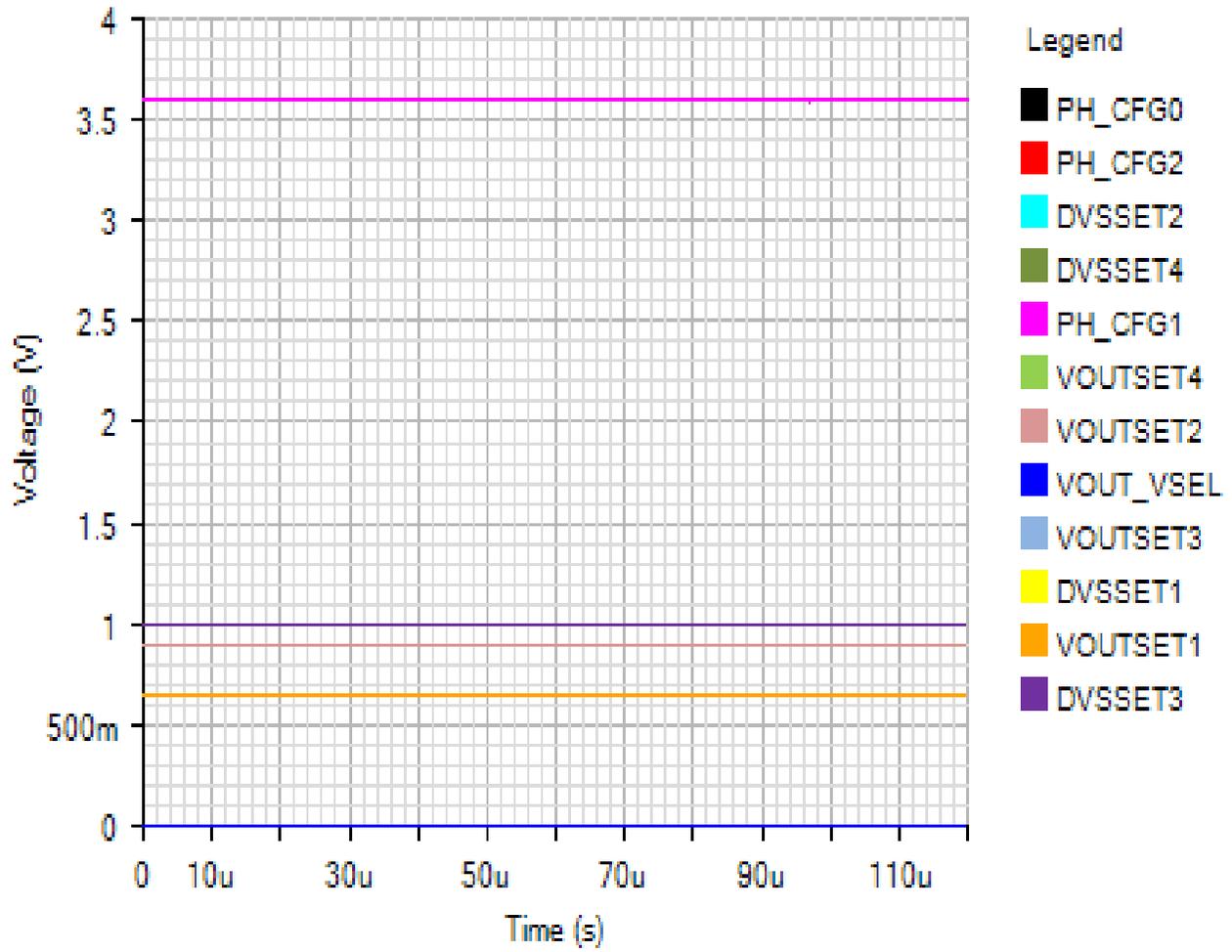


Start Up - Mon Nov 19 2018 17:59:28



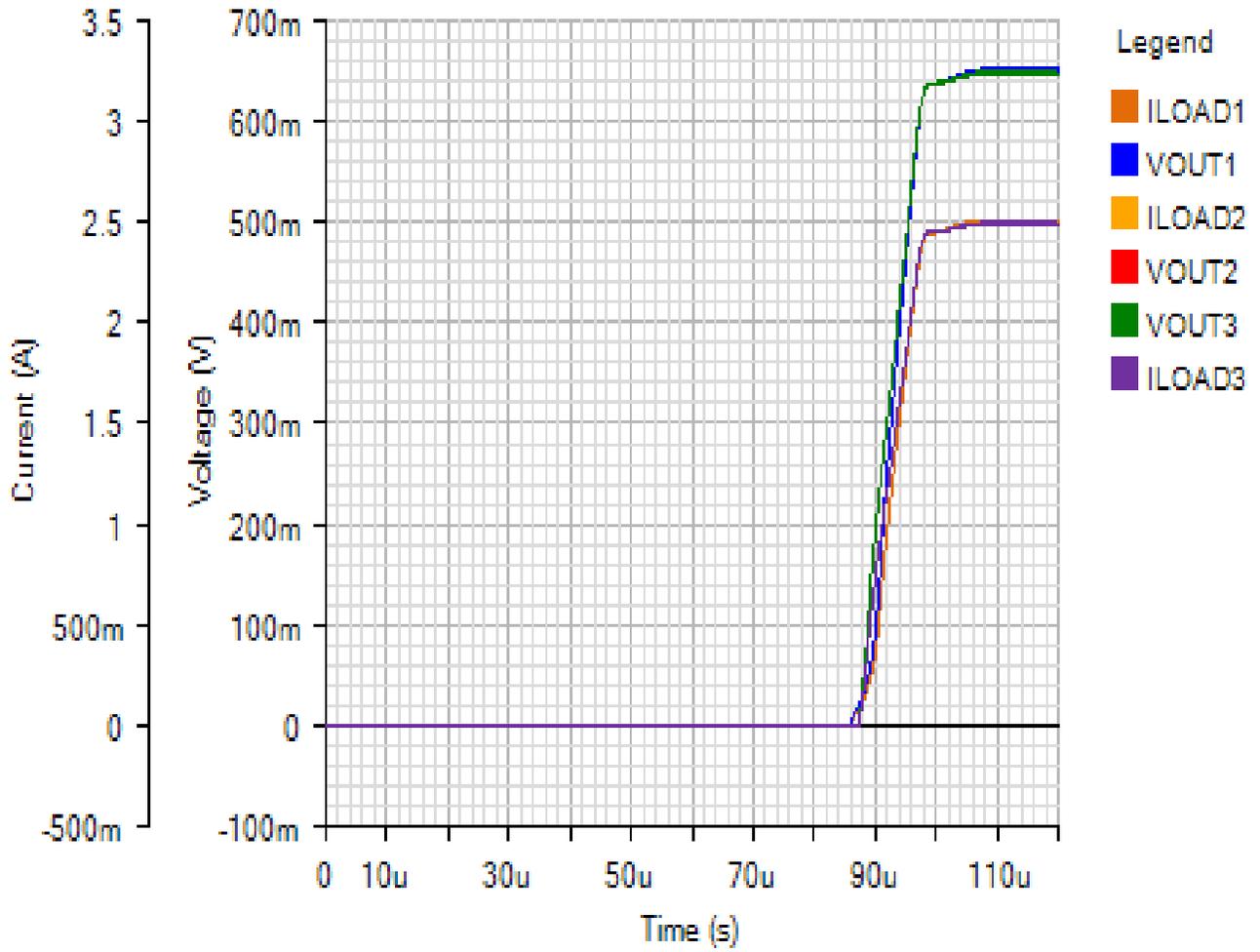
IC

Default



OUTPUT

Default



INPUT

Default

