

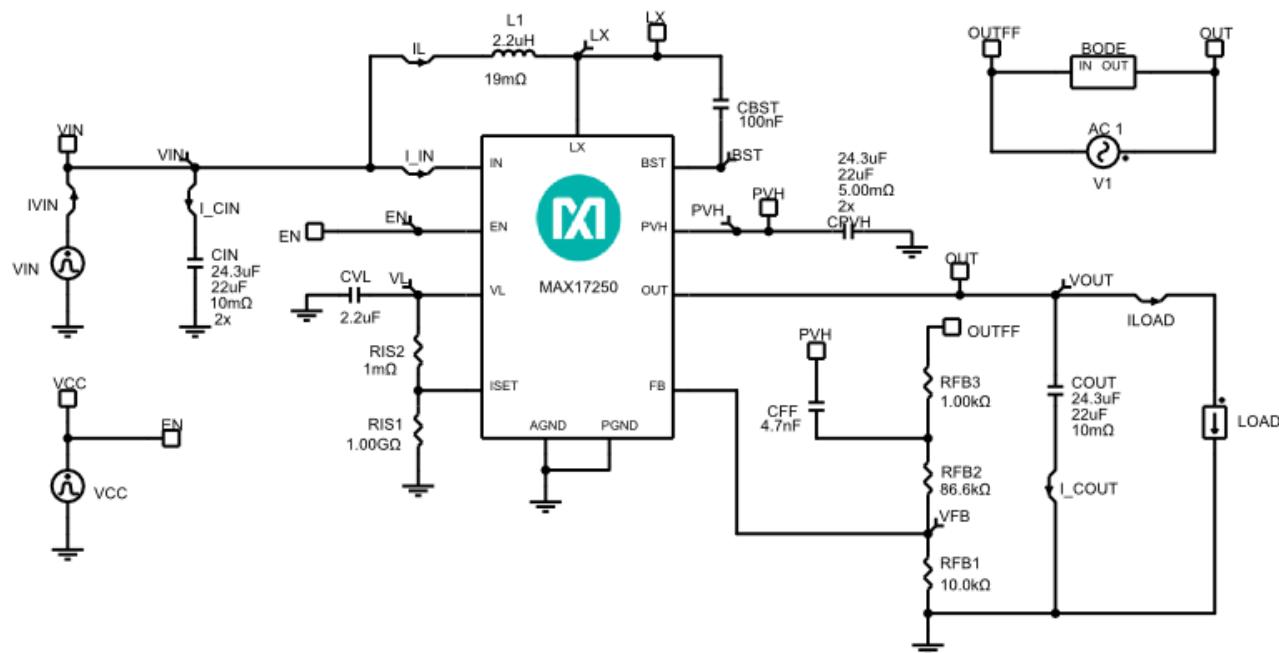
## Initial Design

1.0

## Design Requirements

Parameter	Value
Value	WLP
Minimum Input Voltage	6.2V
Maximum Input Voltage	8.2V
Nominal Input Voltage	7.2V
Output Voltage	12V
Output Current	500mA
BOM Priority	Cost
Ambient Temperature	25°C

## Schematic



Note: If the current level (starting current for Load Steps) is too low, AC, Steady State and Load Step analyses may fail due to PFM mode operation.



## BOM

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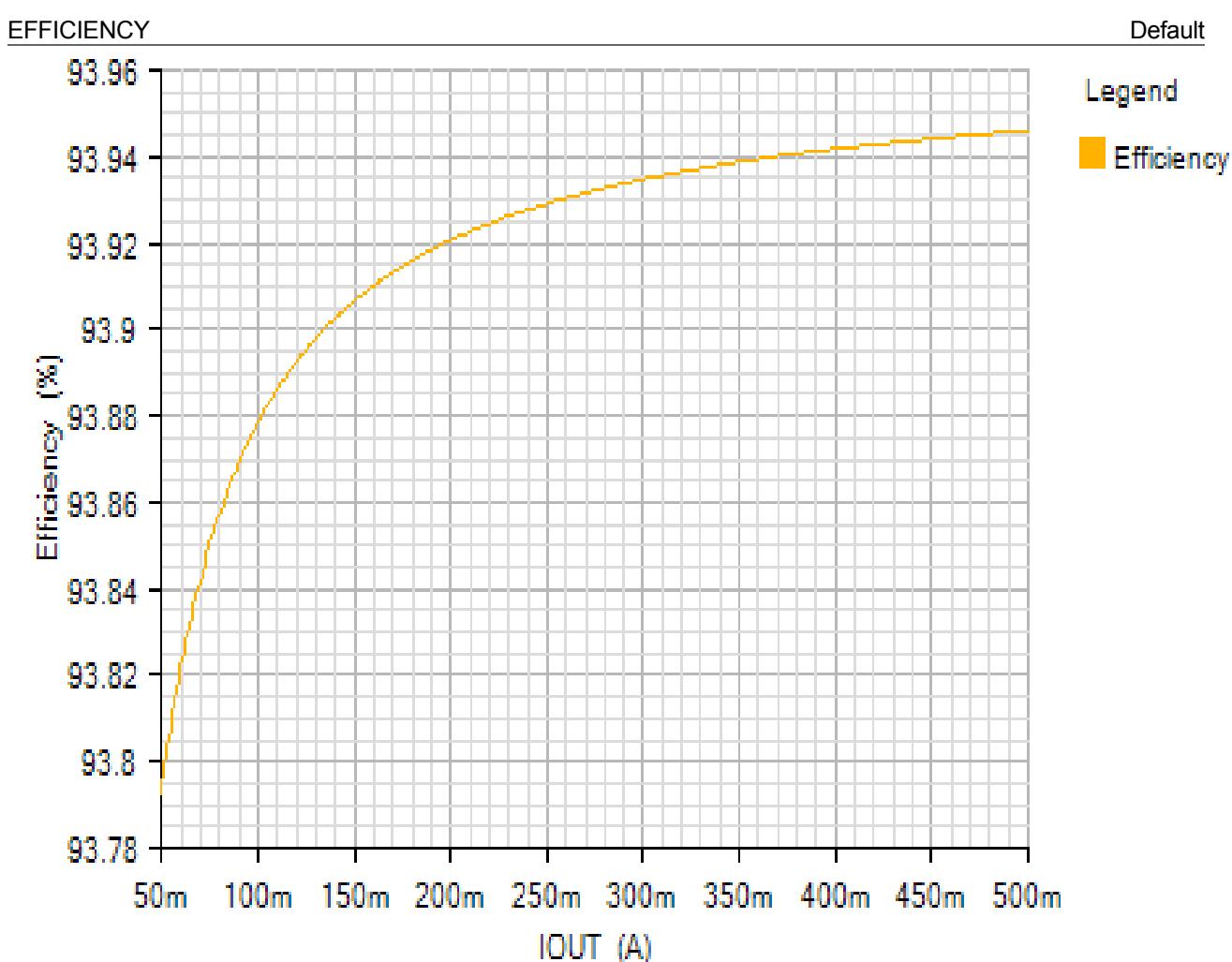
Ref	Qty	Part Number	Manufacturer	Description
U1	1	MAX17250	User-Defined	IC
CBST	1	06035C104KAT2A	AVX	Cap Ceramic 0.1uF 50V X7R 10% Pad SMD 0603 125°C T/R
CFF	1	04023C472KAT2A	AVX	Cap Ceramic 0.0047uF 25V X7R 10% Pad SMD 0402 125°C T/R
CIN	2	GRM32ER71E226ME15	Murata	Cap Ceramic 22uF 25V 1210 125C
COUT	1	GRM32ER71E226ME15	Murata	Cap Ceramic 22uF 25V 1210 125C
CPVH	2	GRM32ER71E226ME15	Murata	Cap Ceramic 22uF 25V 1210 125C
CVL	1	C1608X7R1A225K080AC	TDK	Cap Ceramic 2.2uF 10V X7R 10% Pad SMD 0603 125°C T/R
L1	1	SPM6530T-2R2M	TDK	Inductor Power Shielded Wirewound 2.2uH 20% 100KHz Metal 8.2A 19mOhm DCR T/R
RFB1	1	CPF0603F10KC1	TE Connectivity	Res Thin Film 0603 10K Ohm 1% 0.063W(1/16W) ±50ppm/°C Epoxy Pad SMD T/R
RFB2	1	NTR06F8662CTR	NIC Components	Res Thin Film 0603 86.6K Ohm 1% 0.063W(1/16W) ±25ppm/°C Epoxy Pad SMD T/R
RFB3	1	CPF0603F1K0C1	TE Connectivity	Res Thin Film 0603 1K Ohm 1% 0.063W(1/16W) ±50ppm/°C Epoxy Pad SMD T/R

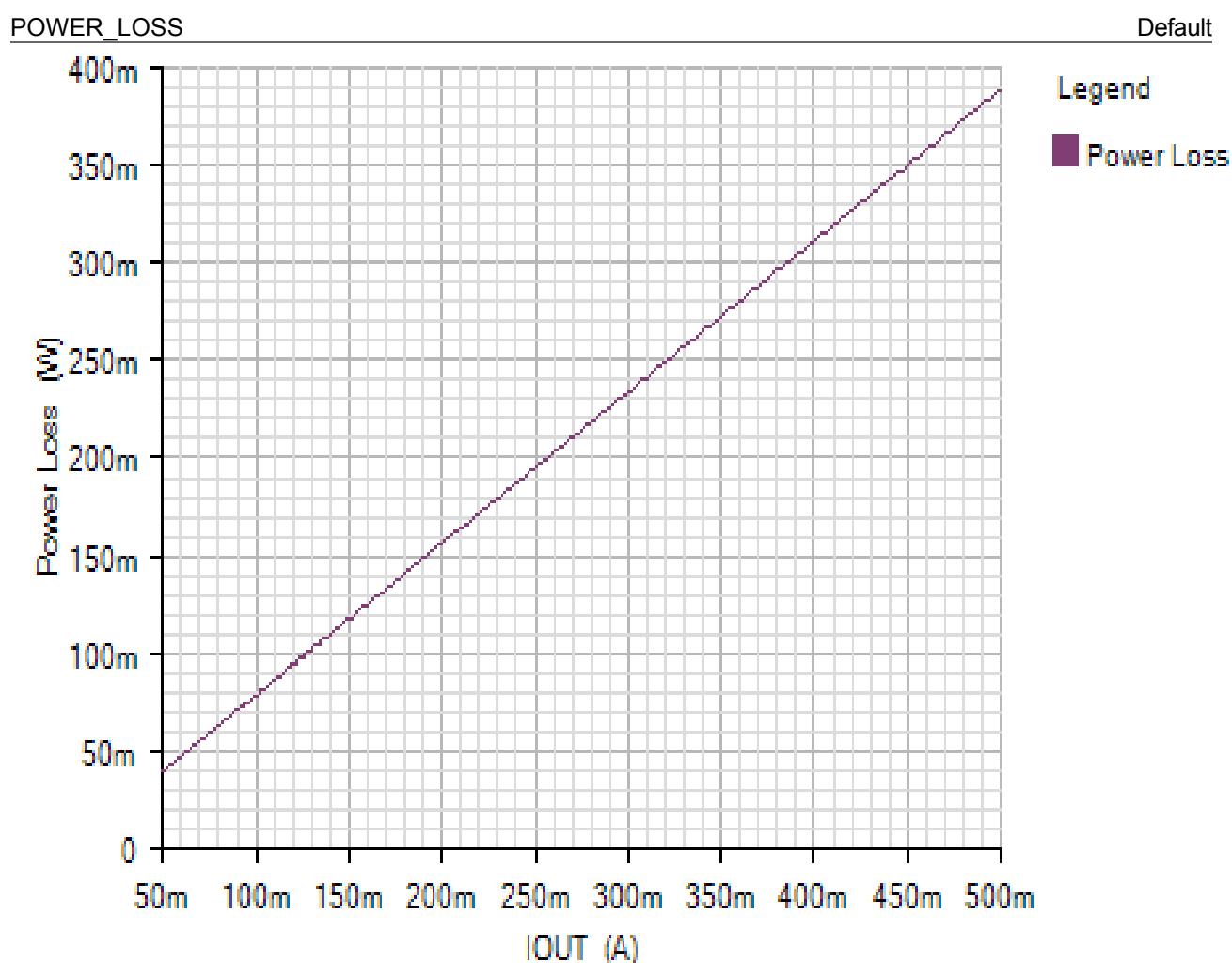
## Simulation Results

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Efficiency - Wed Jan 02 2019 13:57:54

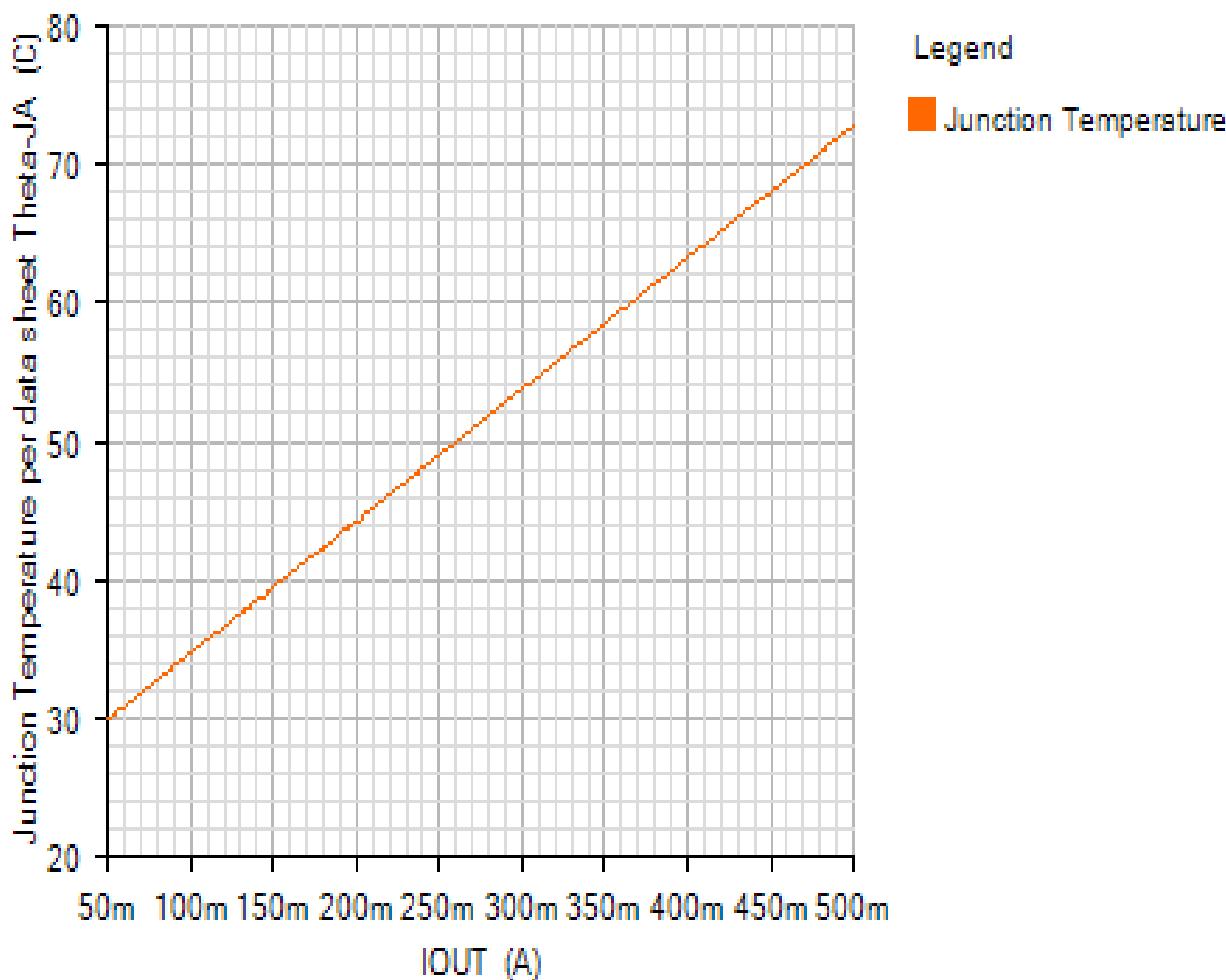
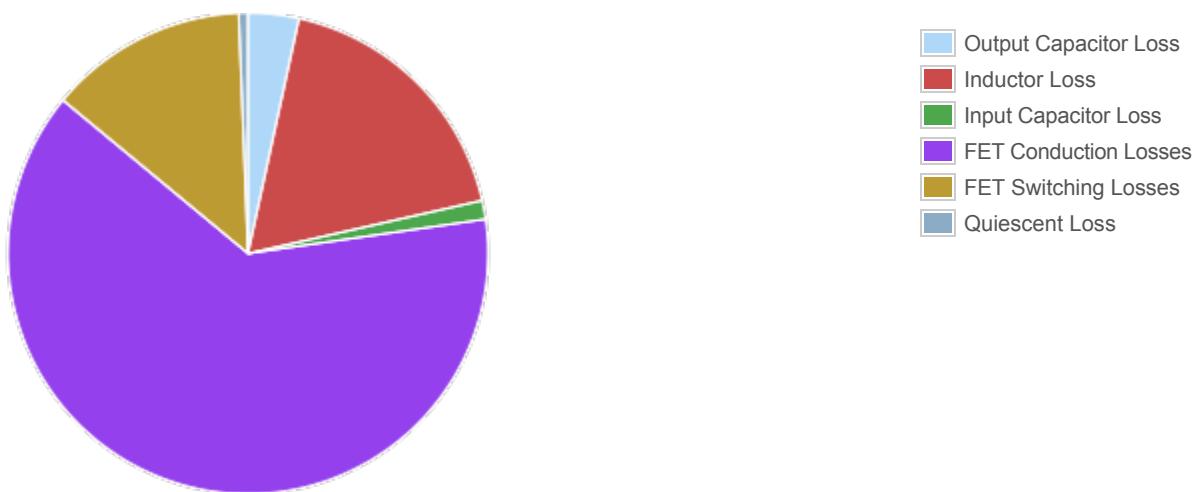
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JUNCTION\_TEMPERATURE

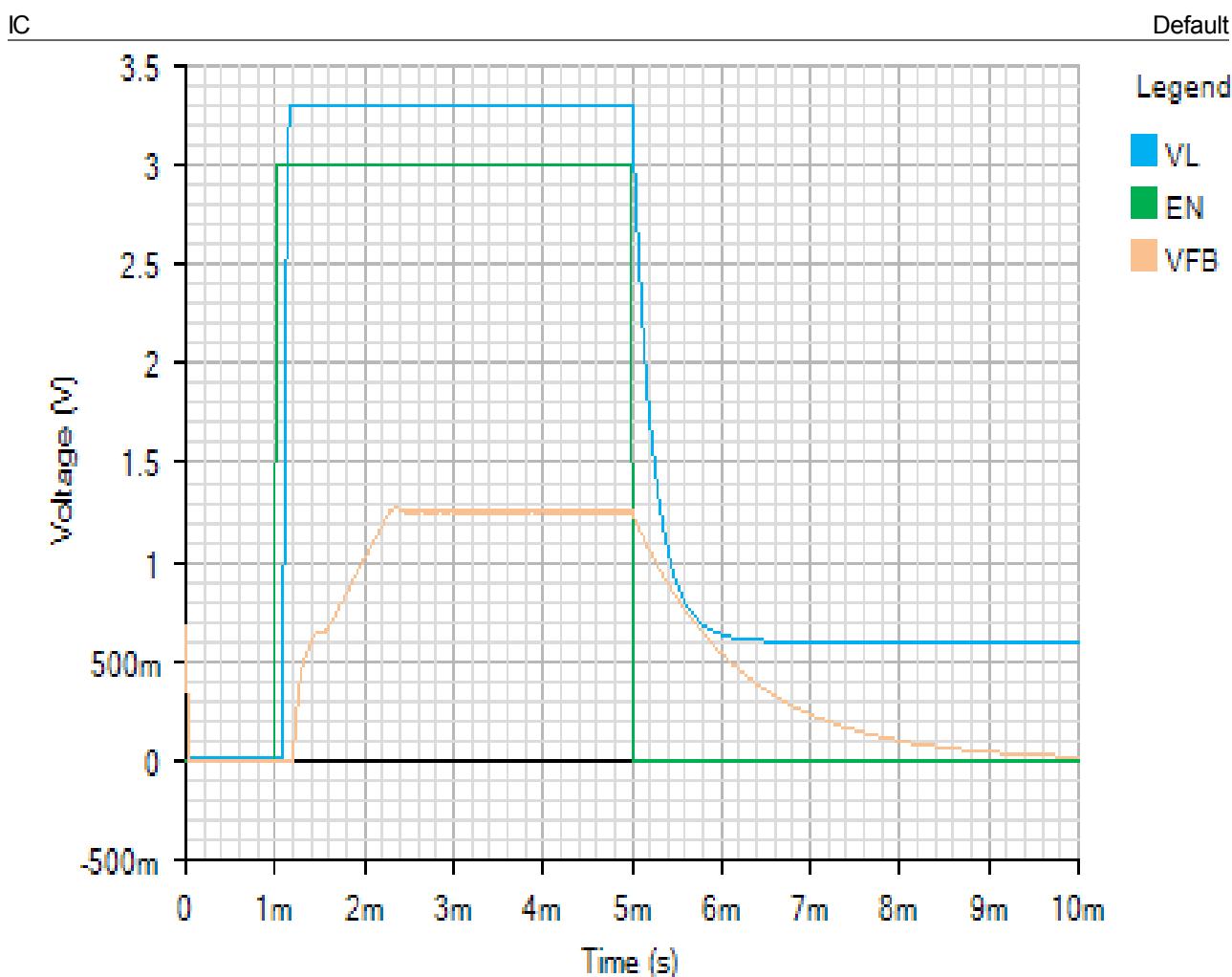
Default

Losses



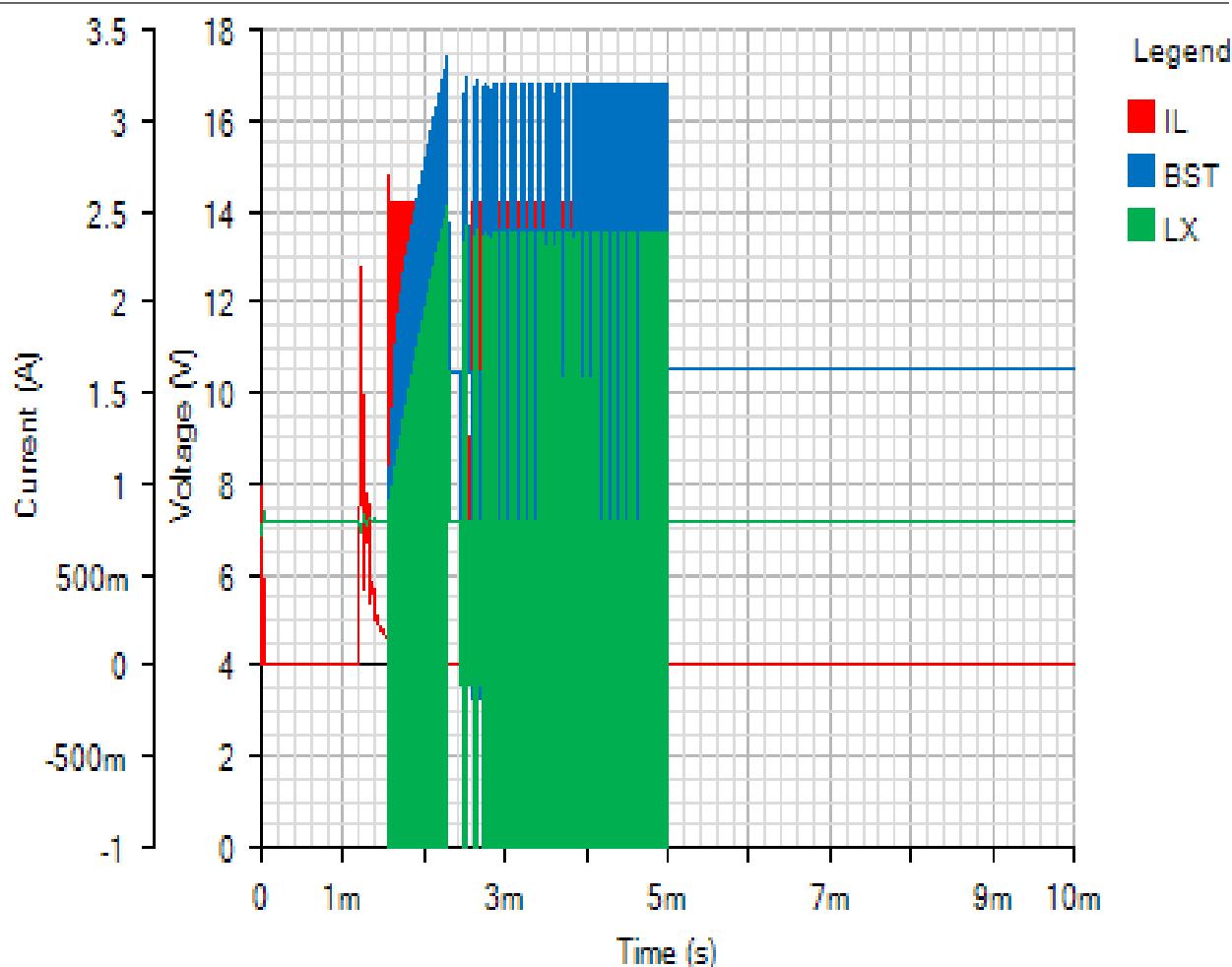
Component	Loss (W)	% of total
Output Capacitor Loss	0.010568	3.4
Inductor Loss	0.05591	18.1
Input Capacitor Loss	0.003894	1.3
FET Conduction Losses	0.195972	63.3
FET Switching Losses	0.041468	13.4
Quiescent Loss	0.00191	0.6
Total	0.309722	100

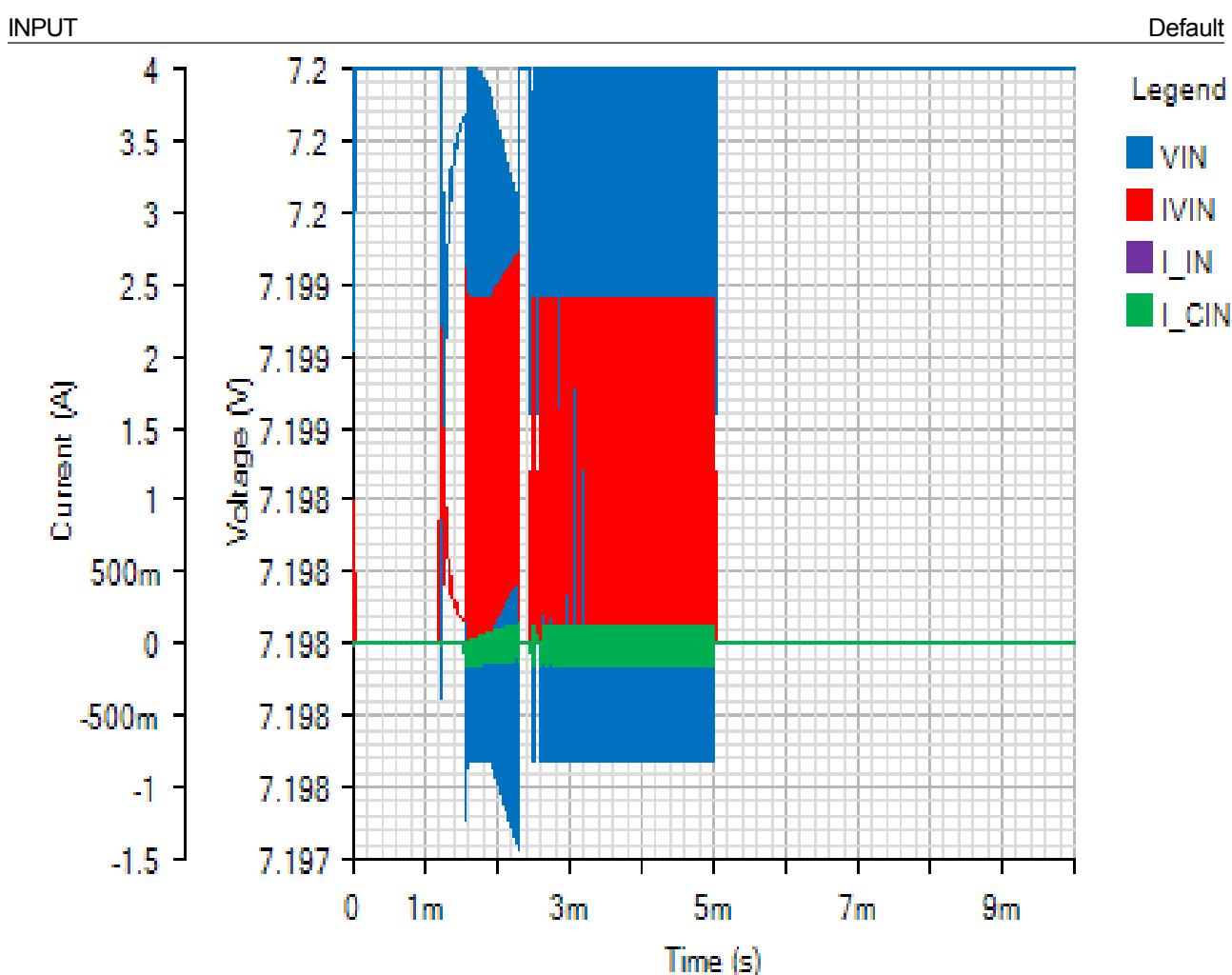
Start Up - Wed Jan 02 2019 13:57:54

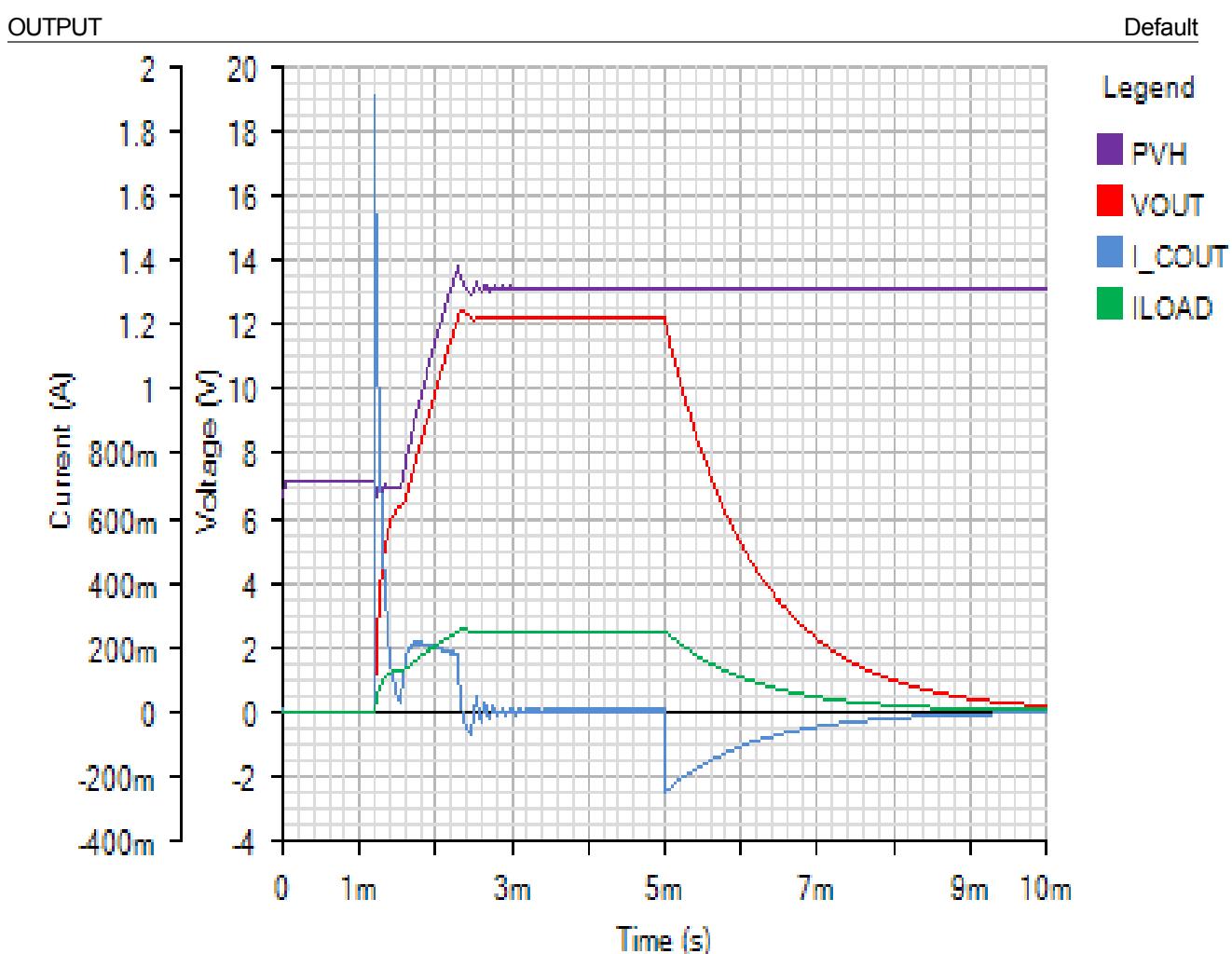


## SWITCHING

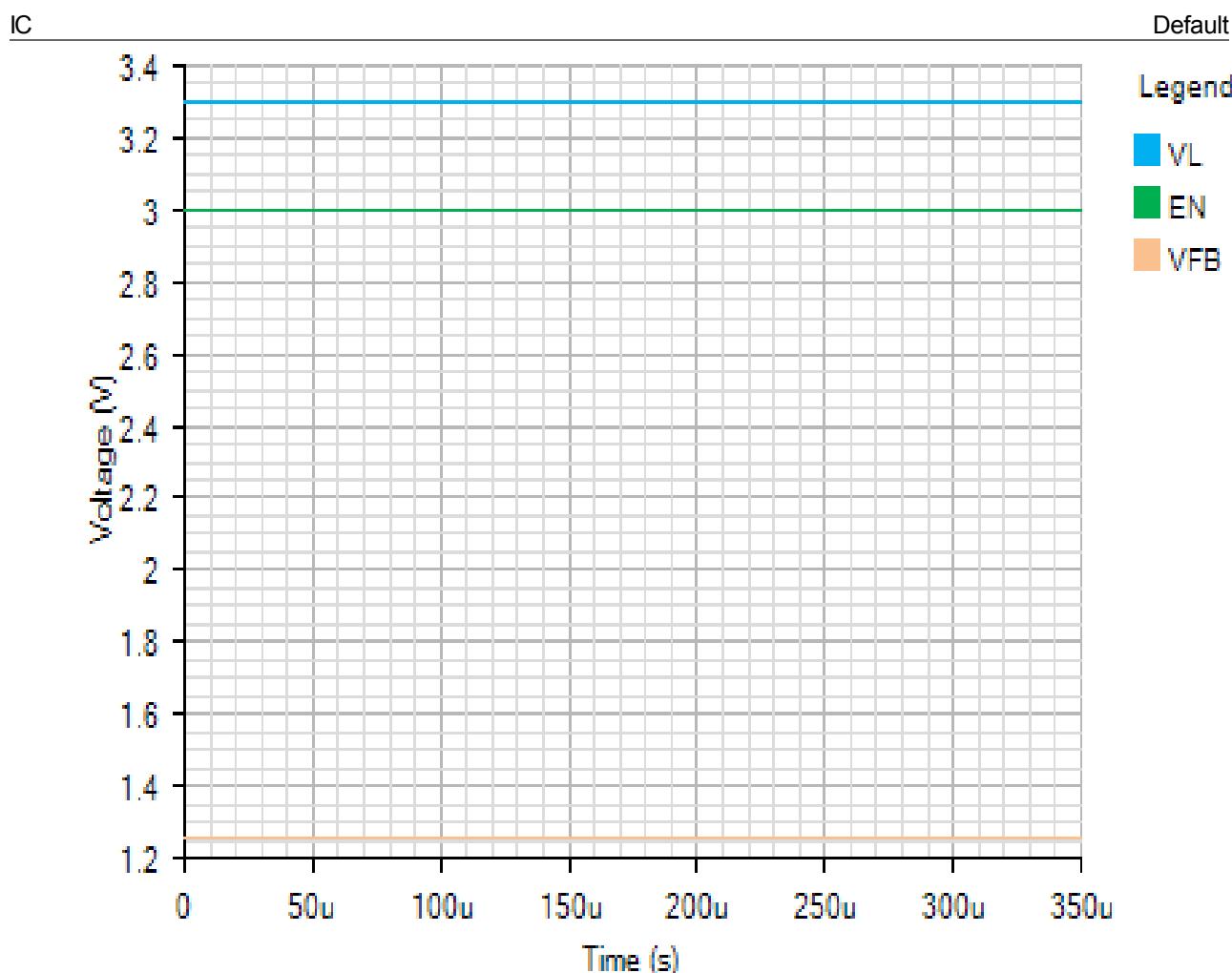
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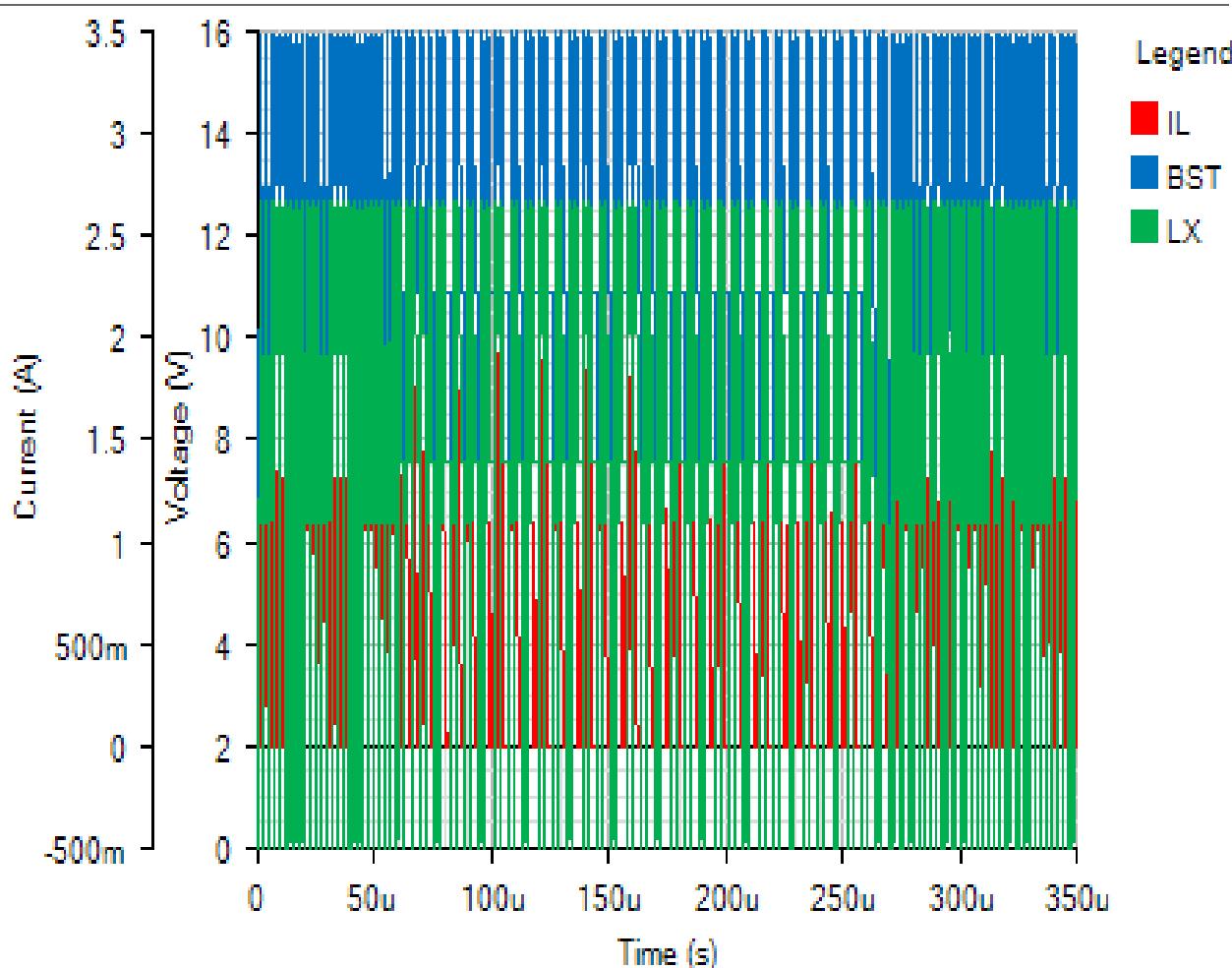


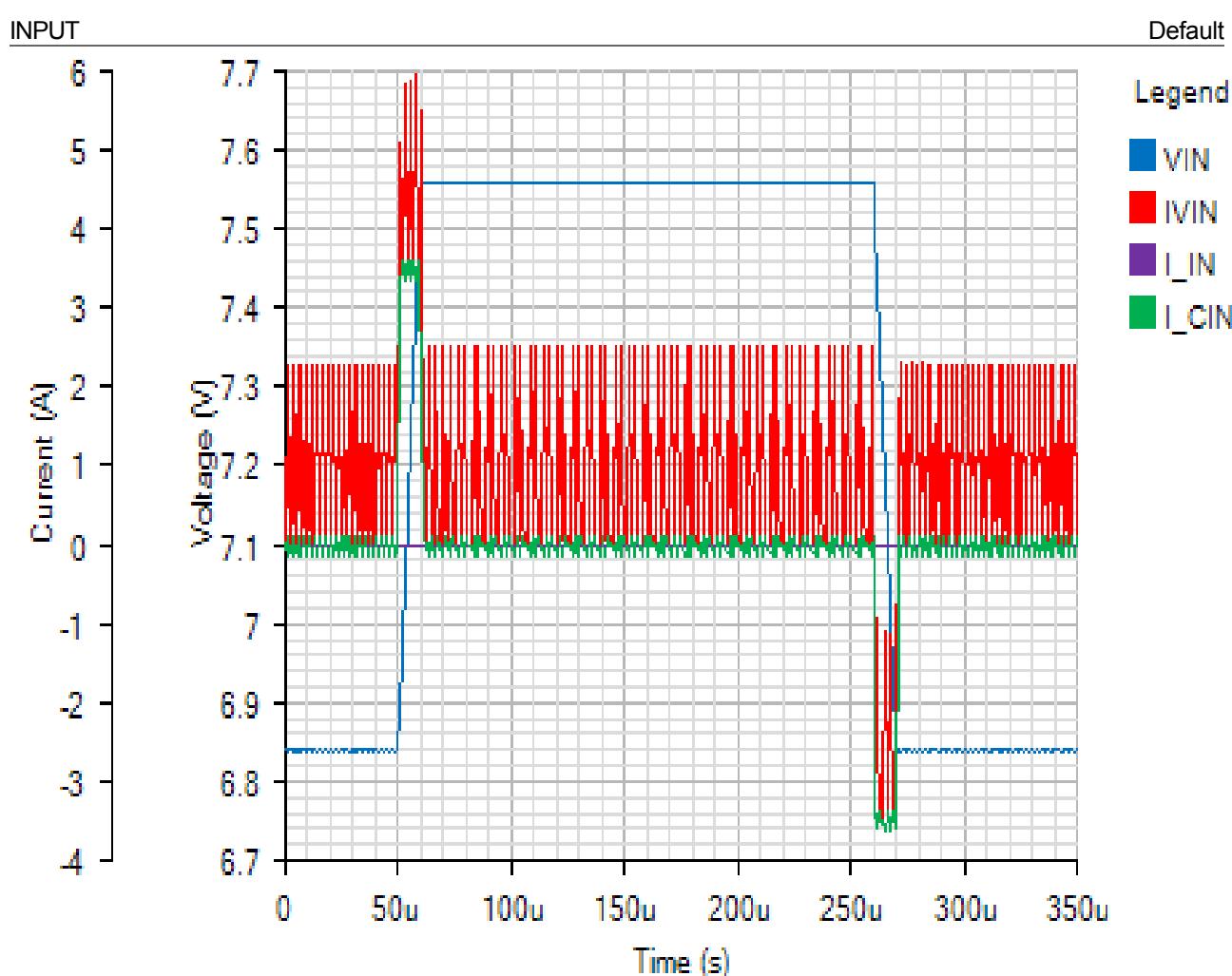
## Line Transient - Wed Jan 02 2019 13:57:54

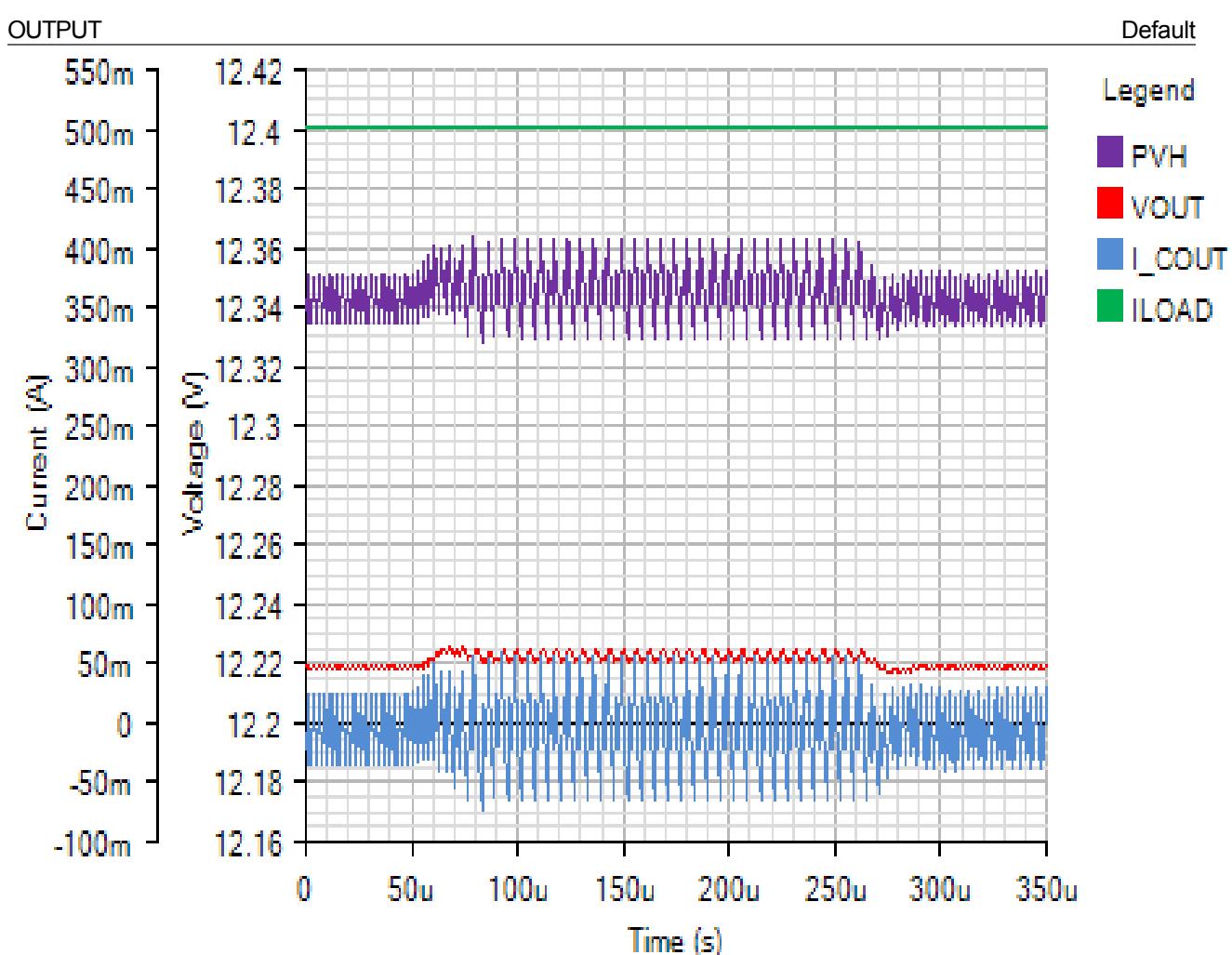


## SWITCHING

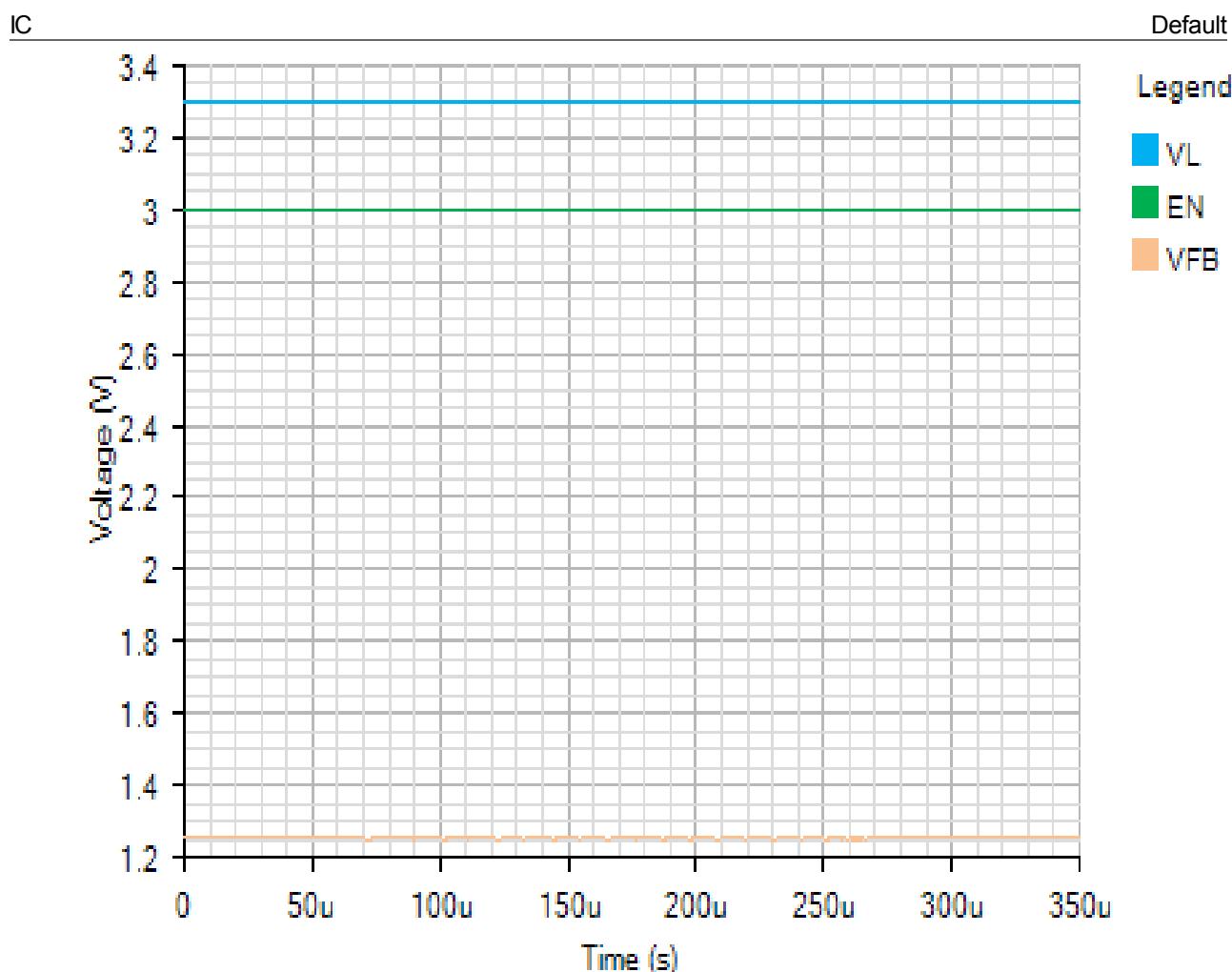
Default





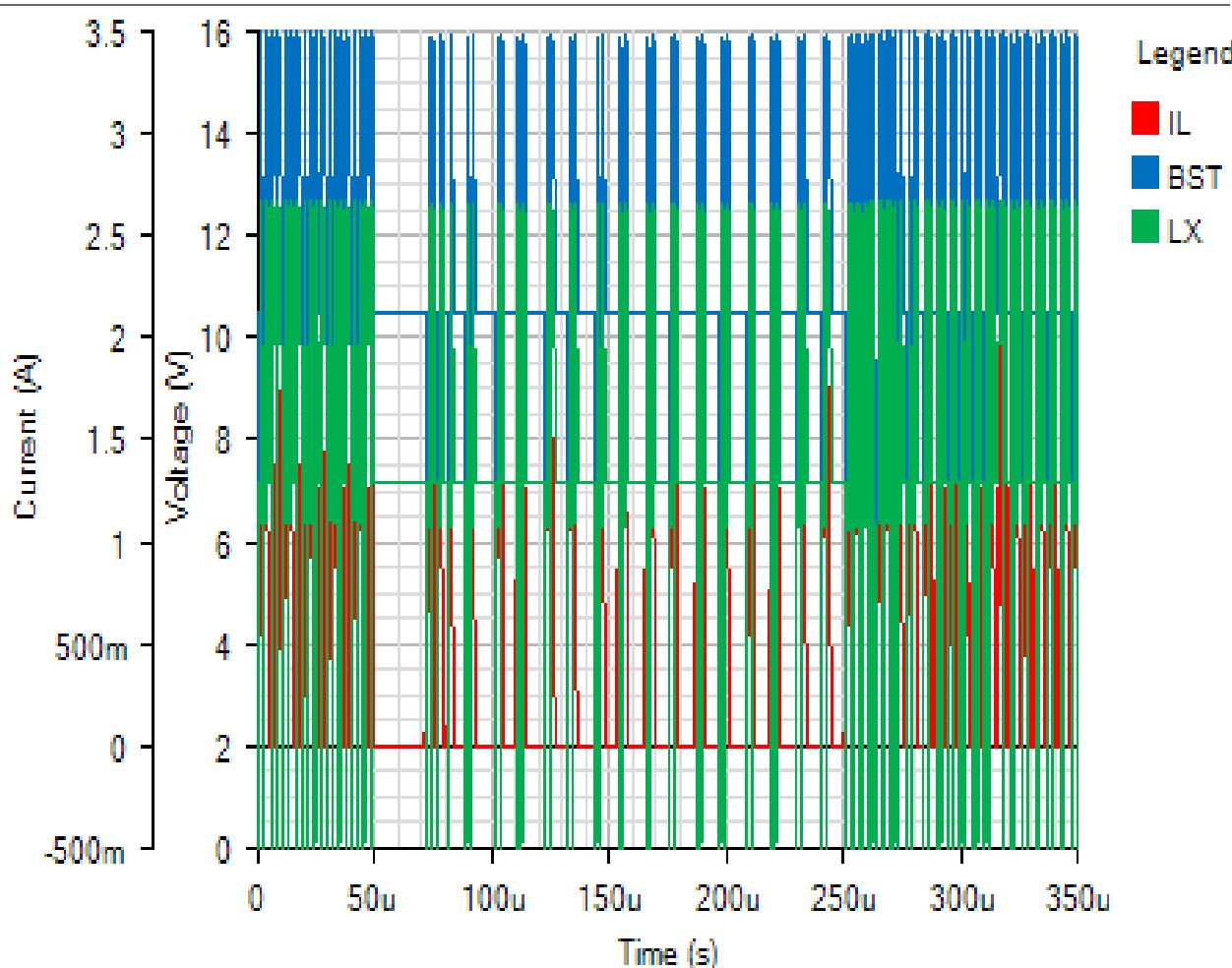


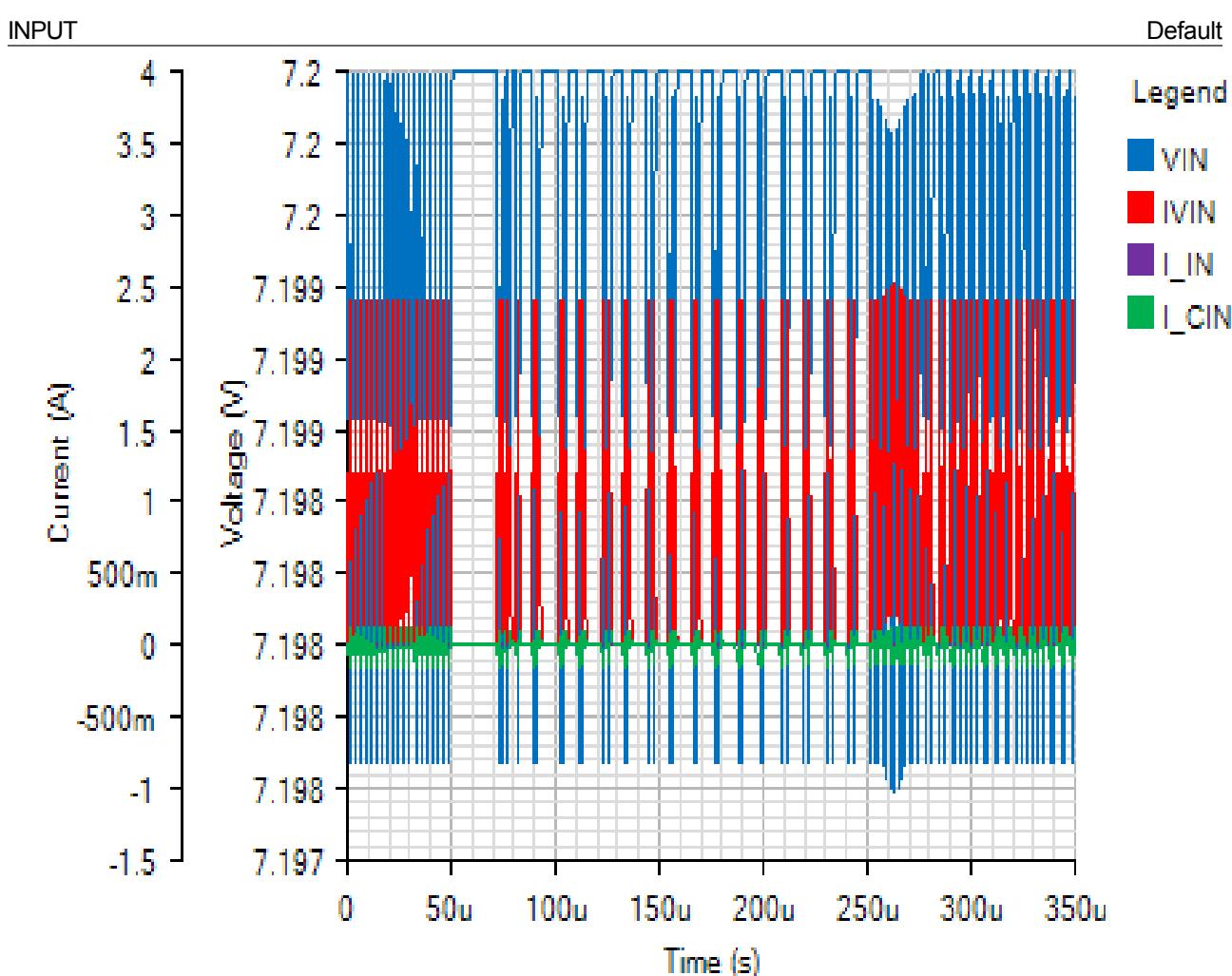
Load Step - Wed Jan 02 2019 13:57:54



SWITCHING

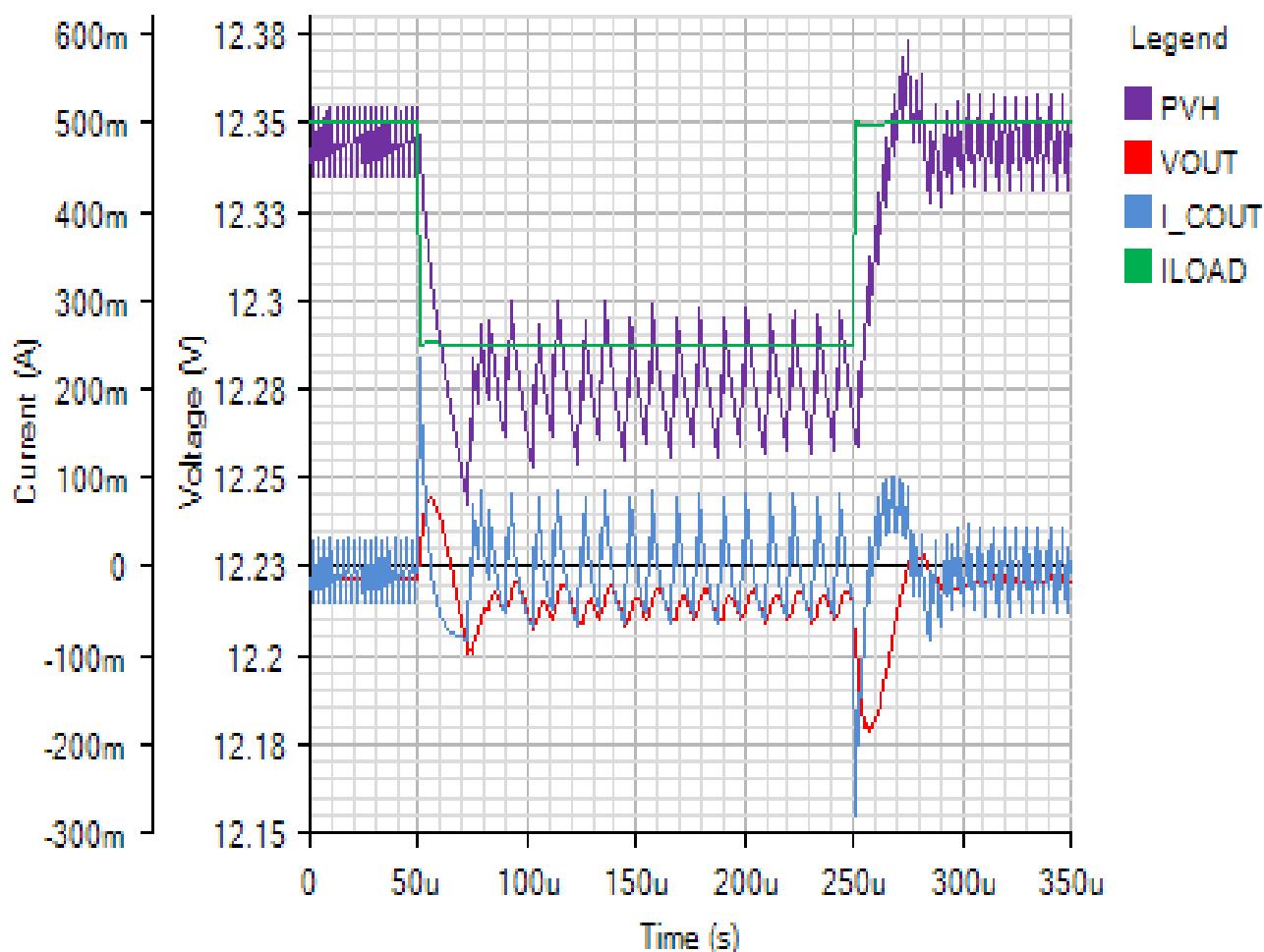
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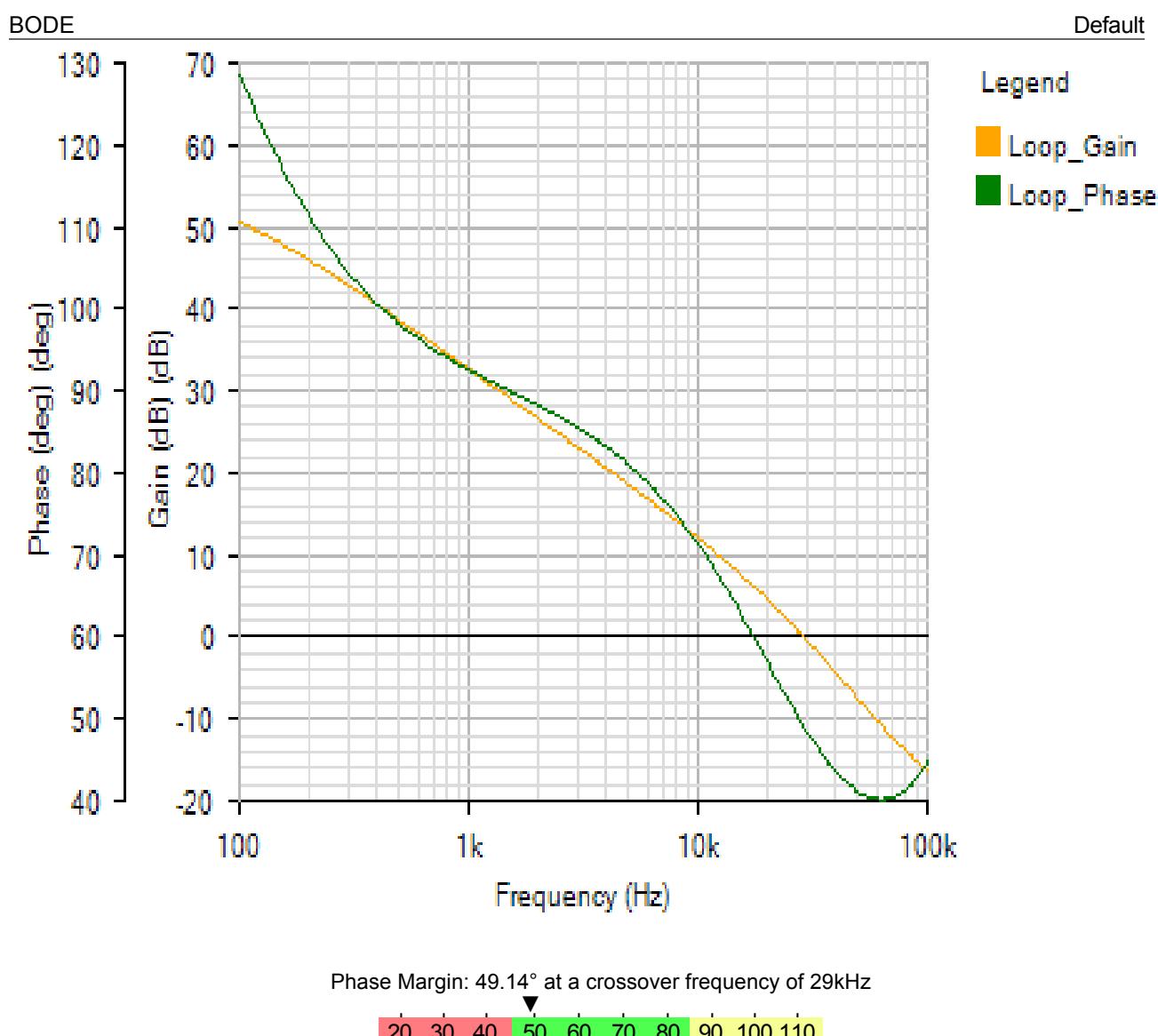


OUTPUT

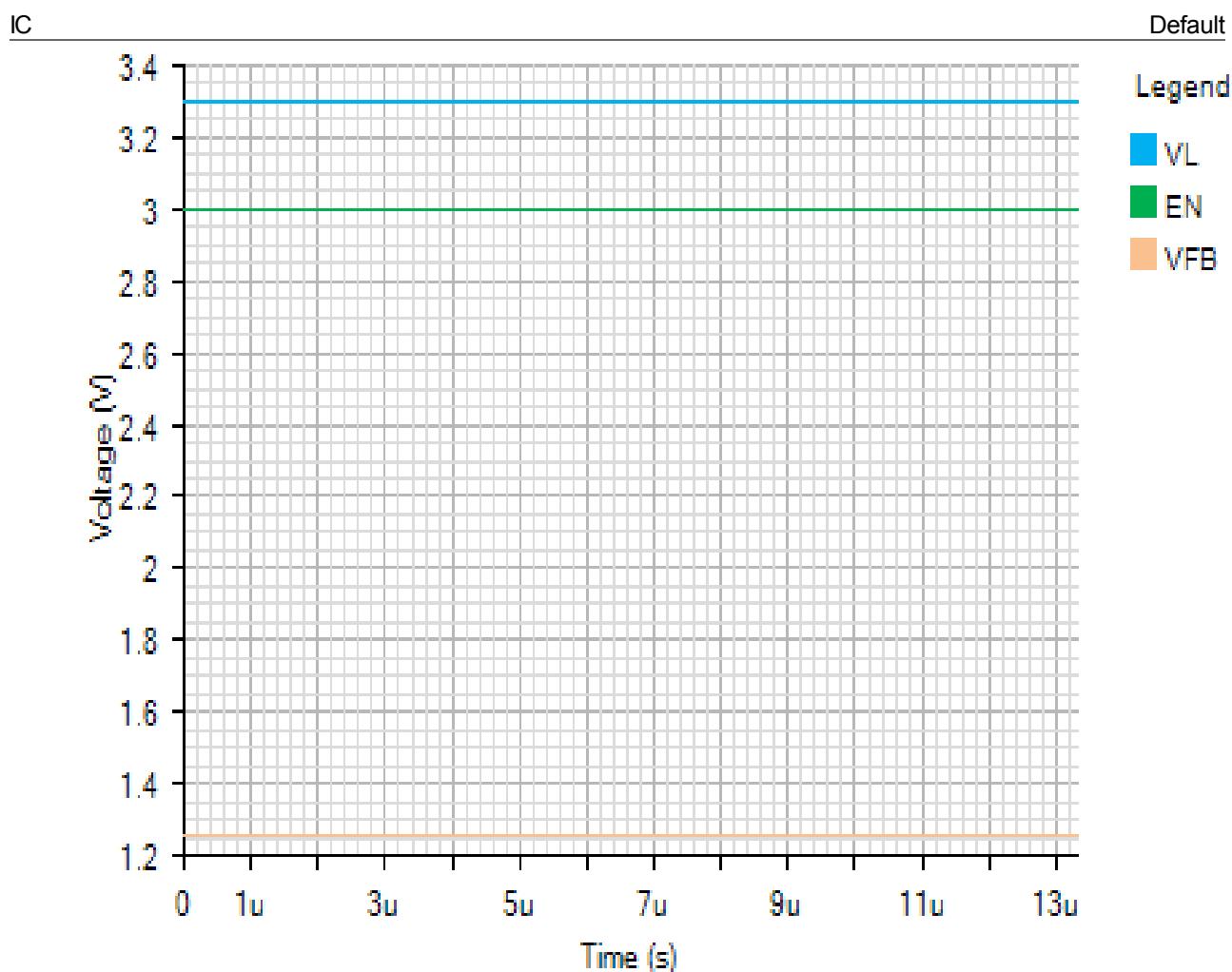
Default



AC Loop - Wed Jan 02 2019 13:57:54

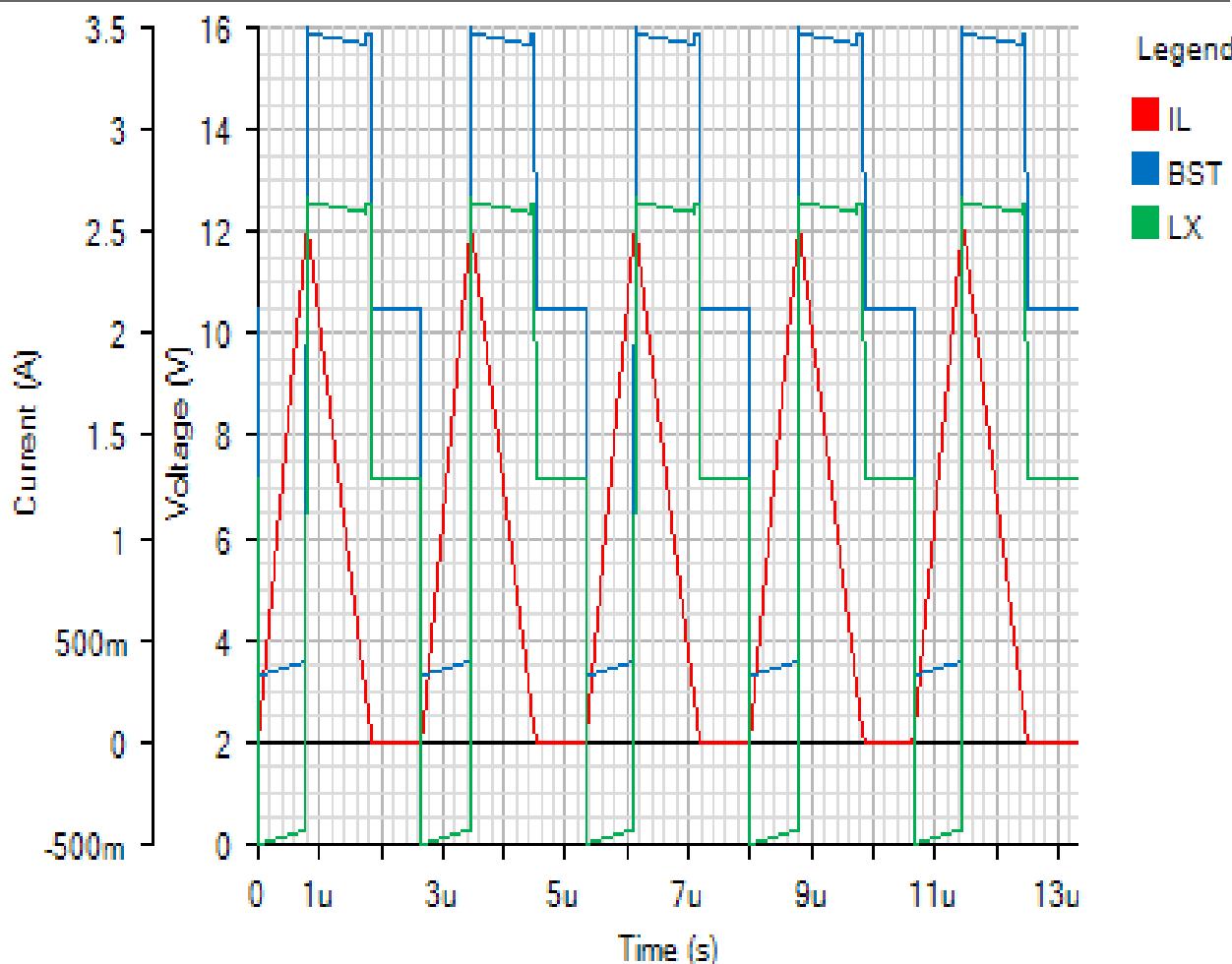


Steady State - Wed Jan 02 2019 13:57:54



## SWITCHING

Default



INPUT

Default

