

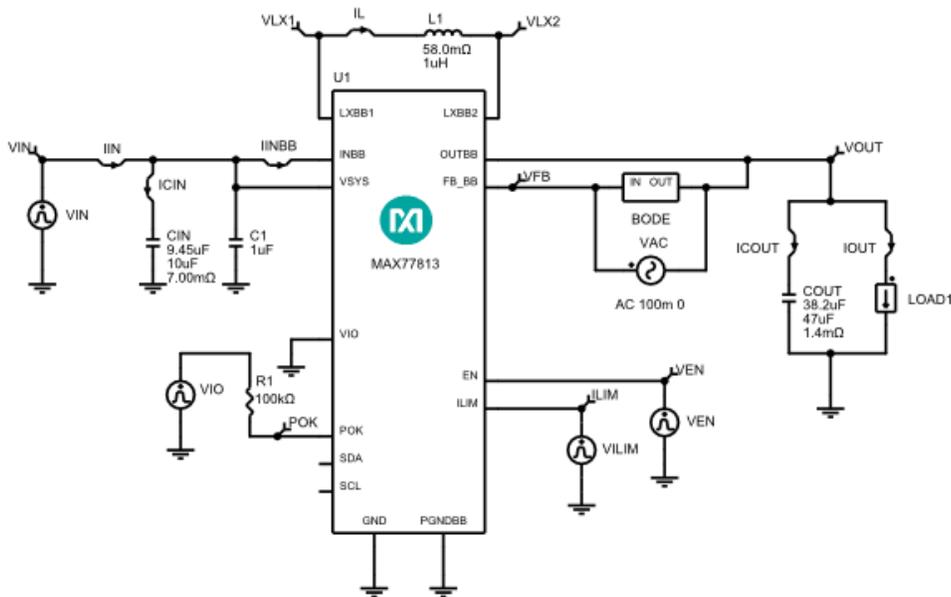
Initial Design

1.0

Design Requirements

Parameter	Value
Minimum Input Voltage	2.5V
Maximum Input Voltage	5.5V
Nominal Input Voltage	5V
Input Voltage Ripple	1%
Output Voltage (Vout)	3.4V
Output Voltage Change	5V
Output Current	2A
Output Voltage Ripple	1%
Performance Priority	Balance Efficiency and Size
BOM Priority	Cost
Mode of Operation	Skip
Inductor Peak Current Limit	4.5A
Output Voltage Ramp-up Slew Rate	20mV/us
Output Voltage Ramp-down Slew Rate	5mV/us
Over Voltage Protection Threshold	1.2
Active Output Discharge	(1==Enable)
Ambient Temperature	25°C

Schematic



*****Notes*****

If the current level (starting current for Load Steps) is too low, AC, Steady State, Load Step and Line Transient analyses may fail.

If the current limit is too close to the output current, simulation may fail as output current might hit the current limit during the start

BOM

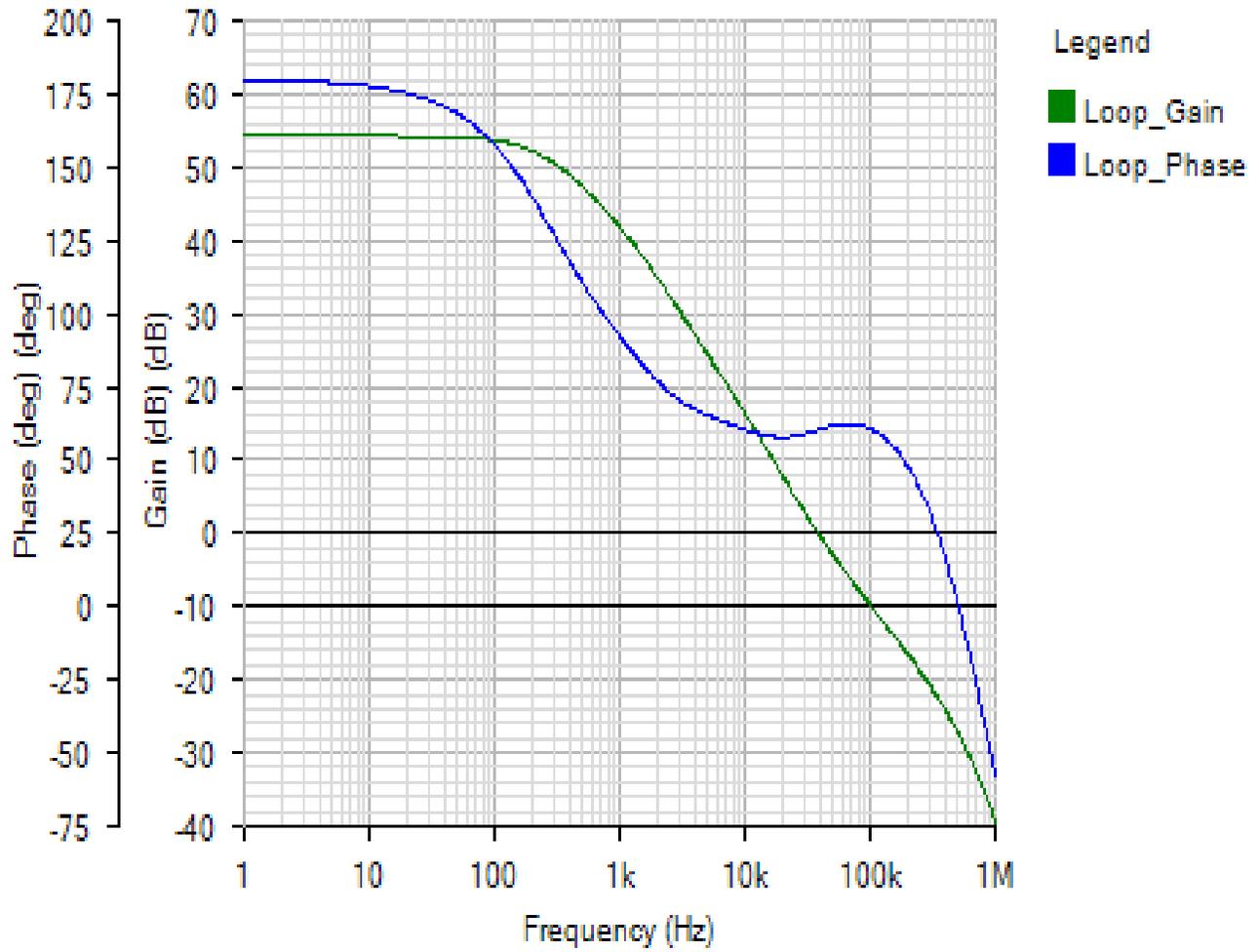
Ref	Qty	Part Number	Manufacturer	Description
U1	1	MAX77813	User-Defined	IC
C1	1	CC0402KRX5R5BB105	Yageo	Cap Ceramic 1uF 6.3V X5R 10% Pad SMD 0402 85°C T/R
CIN	1	C1206C106K9PAC	Kemet	Cap Ceramic 10uF 6.3V X5R 10% SMD 1206 85C Bulk
COUT	1	GRM32ER60J476ME20L	Murata	Cap Ceramic 47uF 6.3V X5R 20% SMD 1210 85C Embossed T/R
L1	1	HMLE20161B-1R0MDR	Cyntec	Inductor 1uH 48mOhm 3.34A Isat 2.7A Irms
R1	1	ERJ2GEJ104X	Panasonic	Res Thick Film 0402 100K Ohm 5% 0.1W(1/10W) ±200ppm/°C Pad SMD Automotive T/R

Simulation Results

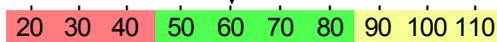
AC Loop - Wed Feb 13 2019 09:32:21

BODE

Default



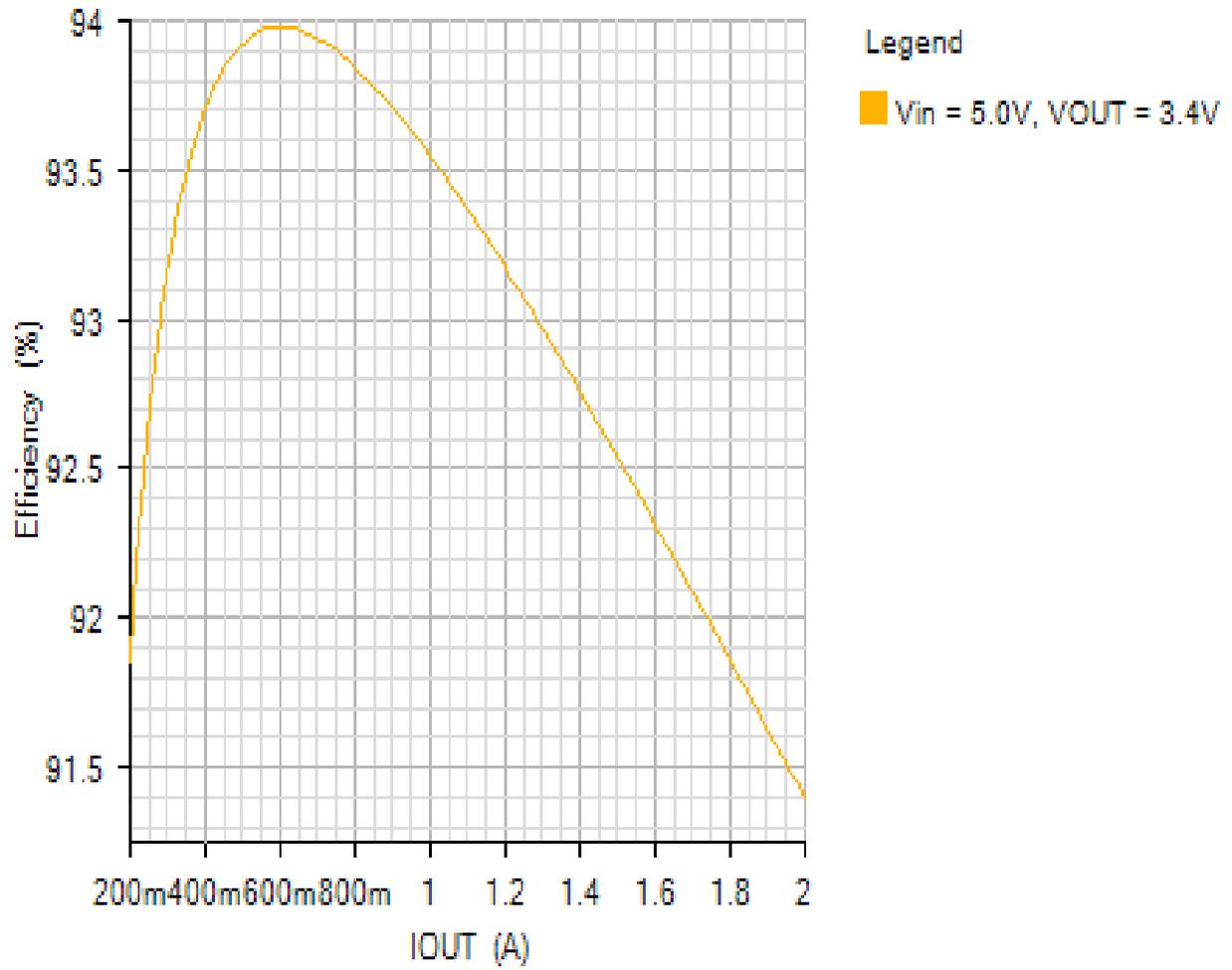
Phase Margin: 60.35° at a crossover frequency of 38.6kHz



Efficiency - Wed Feb 13 2019 09:32:21

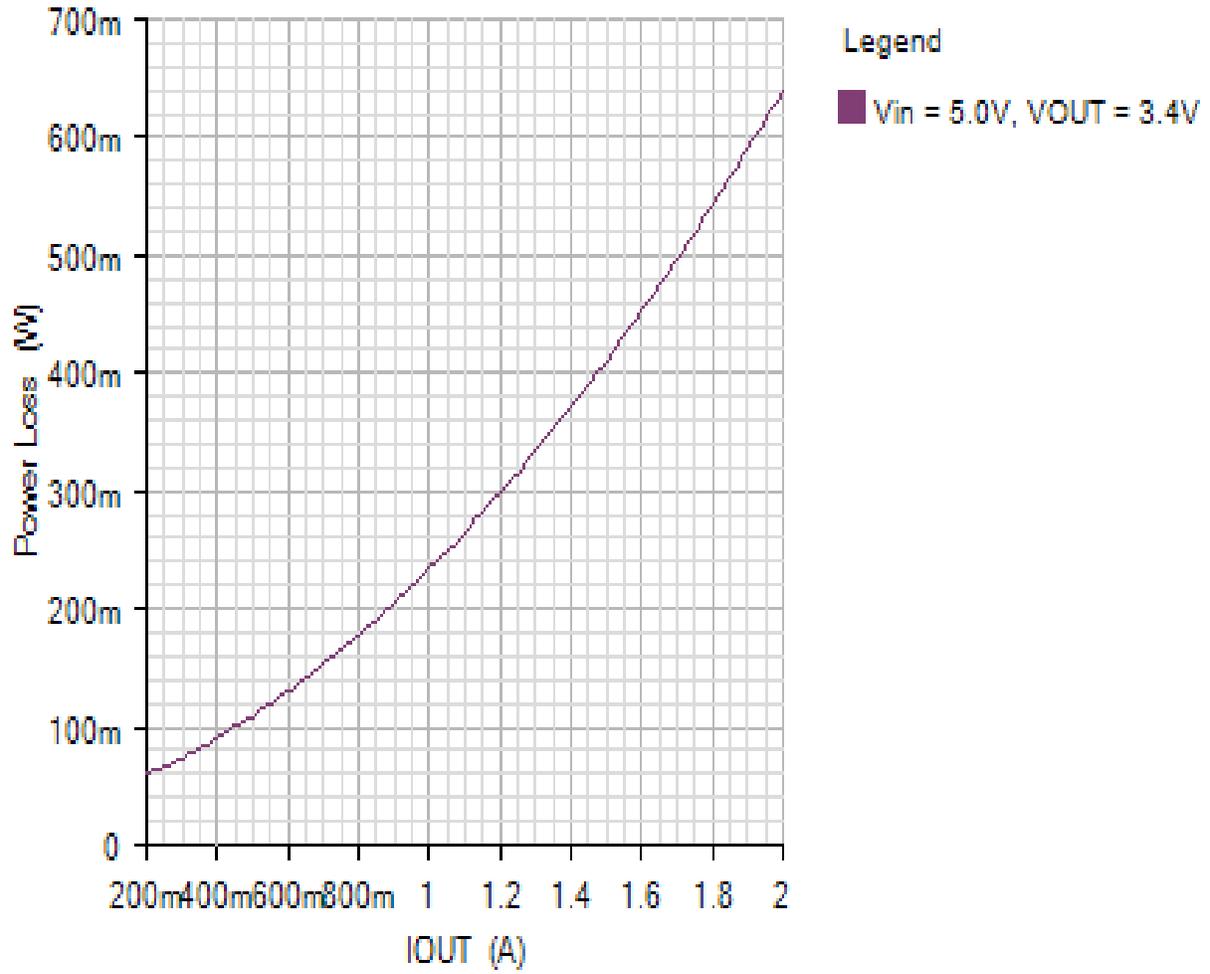
EFFICIENCY_PLOT

Default



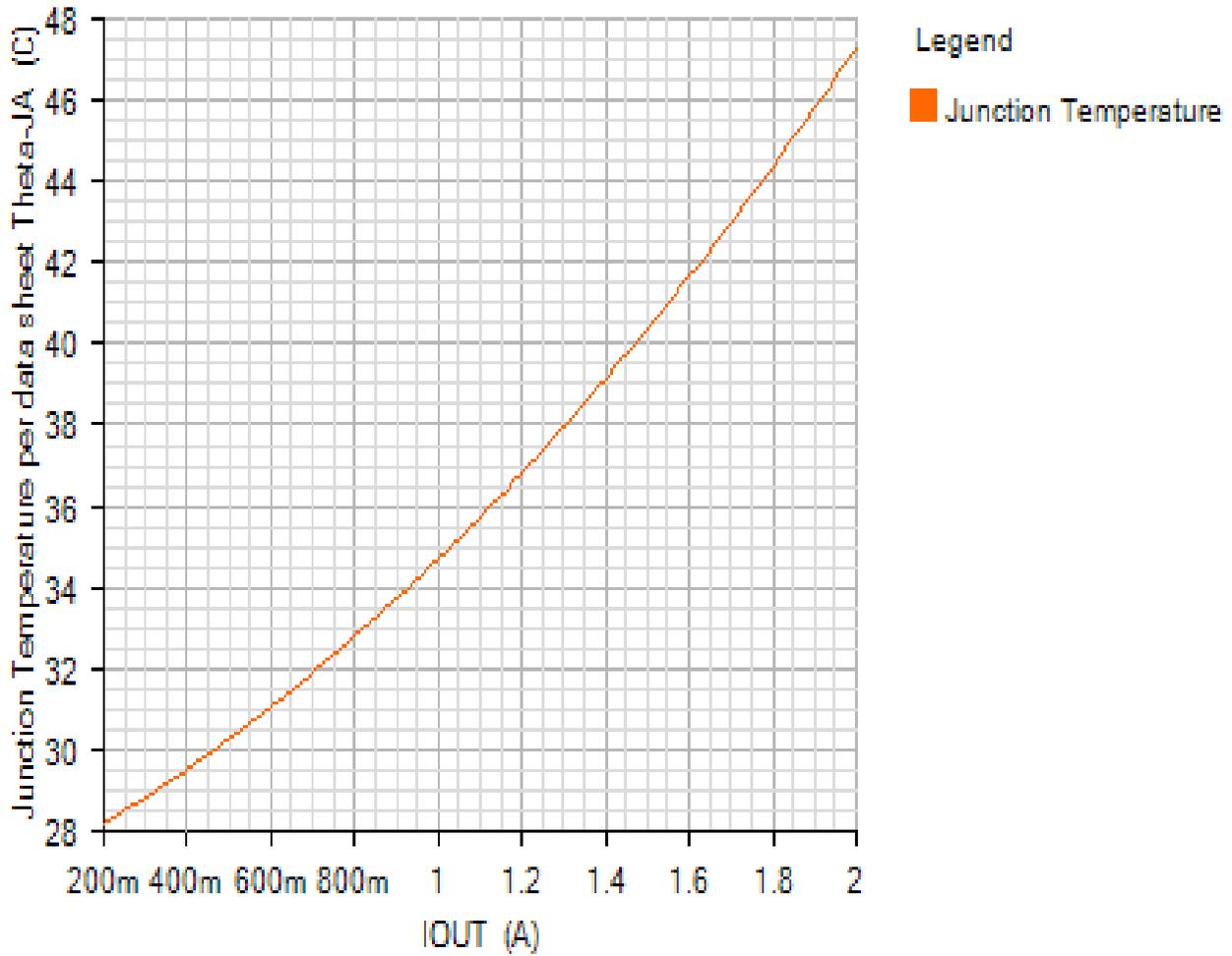
POWER_LOSS_PLOT

Default

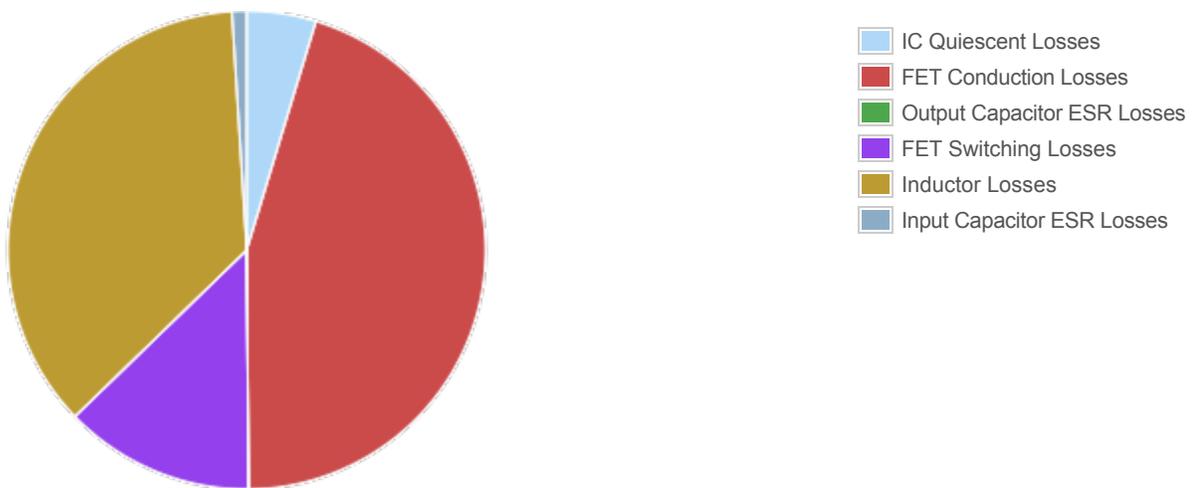


JUNCTION_TEMPERATURE_PLOT

Default



Losses



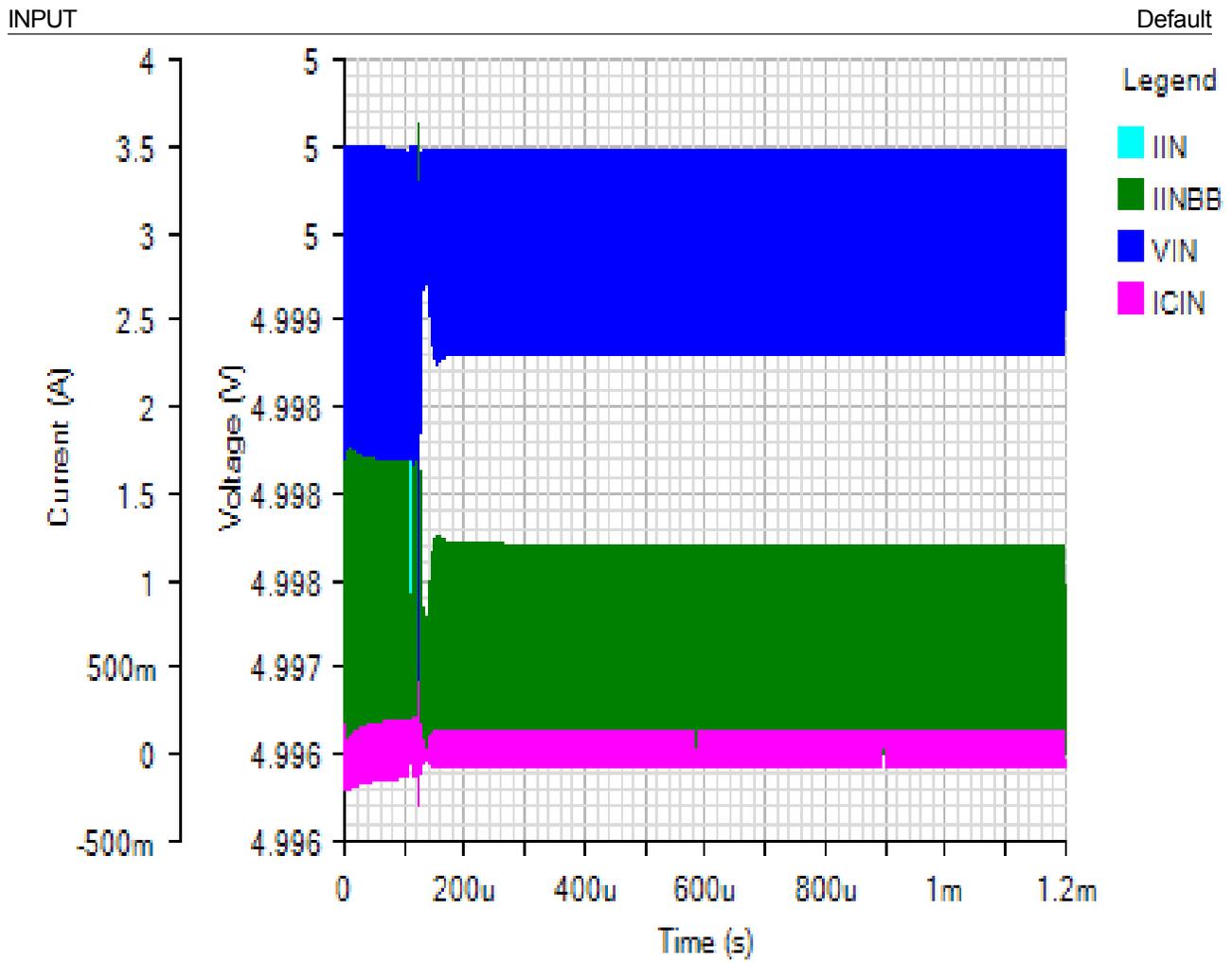
Component

Loss (W)

% of total

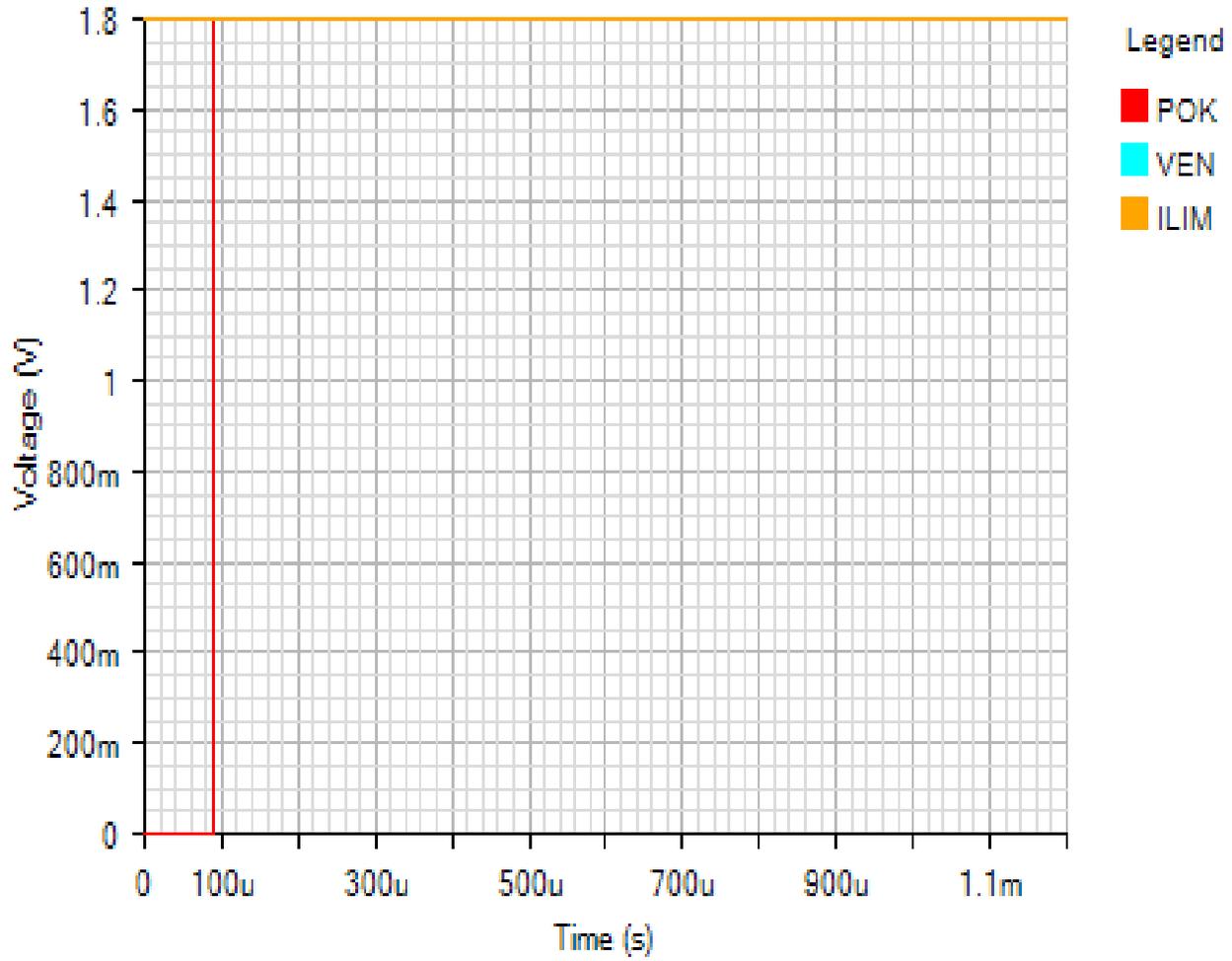
Component	Loss (W)	% of total
IC Quiescent Losses	0.046871	4.7
FET Conduction Losses	0.45184	45.2
Output Capacitor ESR Losses	0.000035	0
FET Switching Losses	0.128896	12.9
Inductor Losses	0.362472	36.2
Input Capacitor ESR Losses	0.009886	1
Total	1	100

Start Up - Wed Feb 13 2019 09:32:21



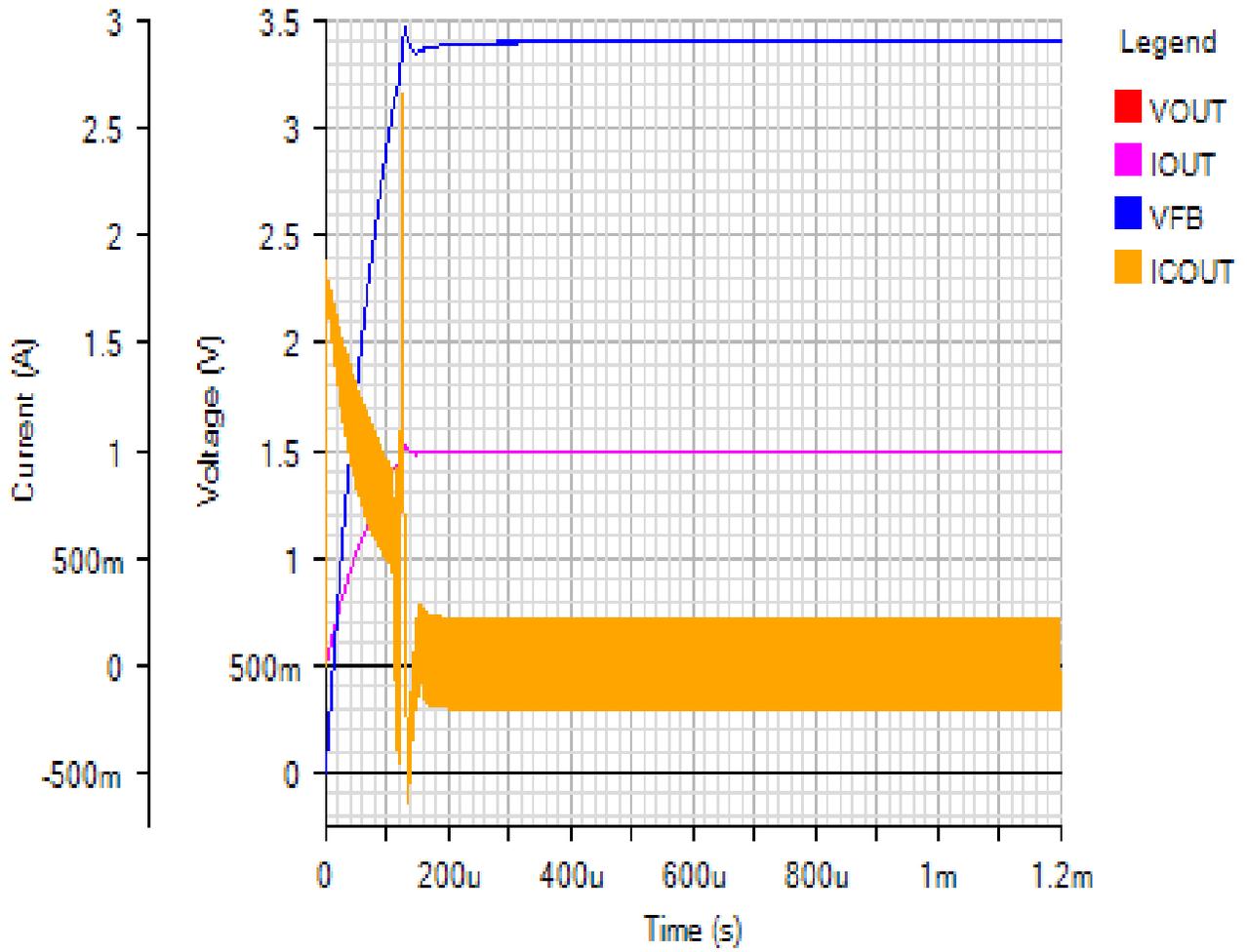
IC

Default



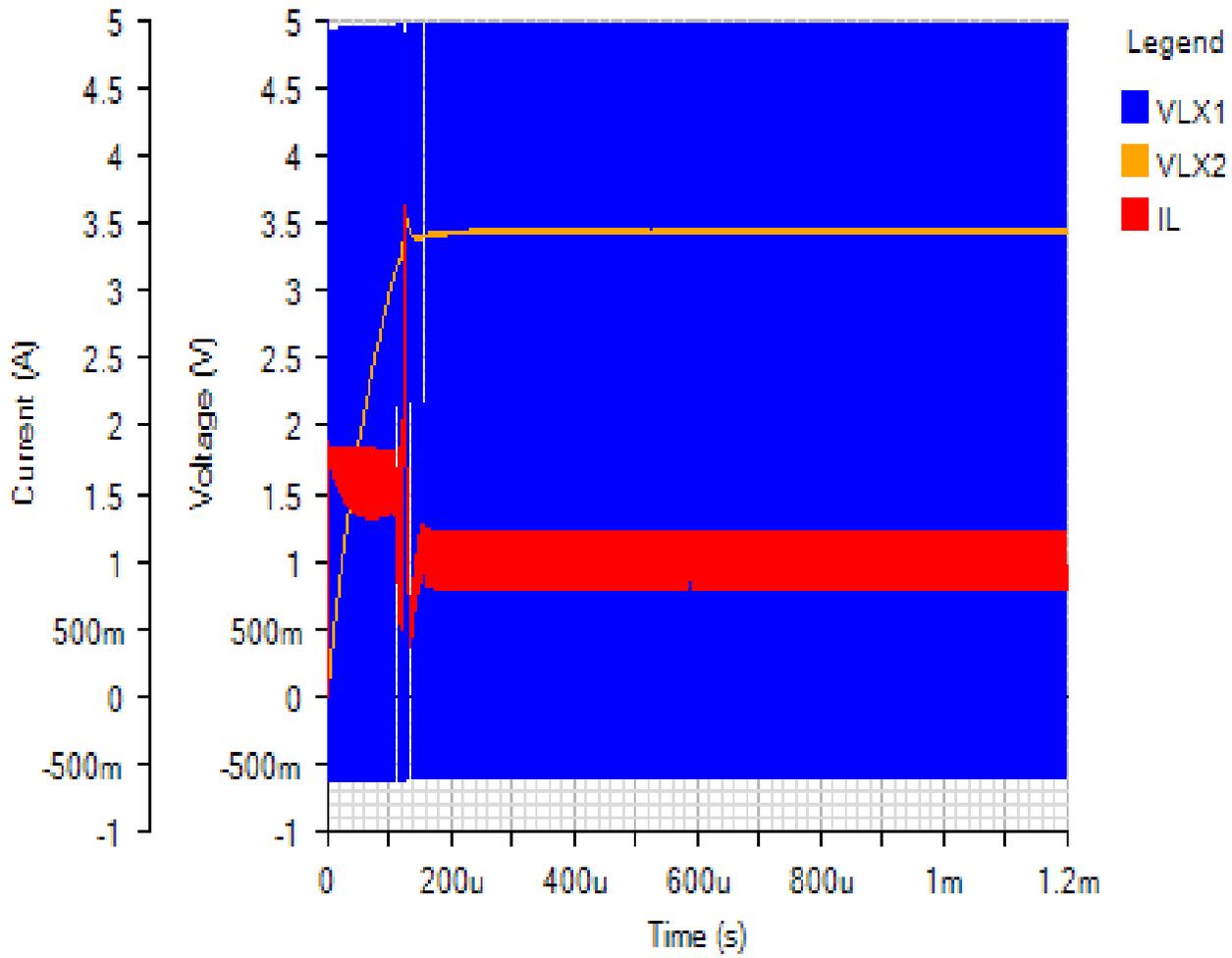
OUTPUT

Default

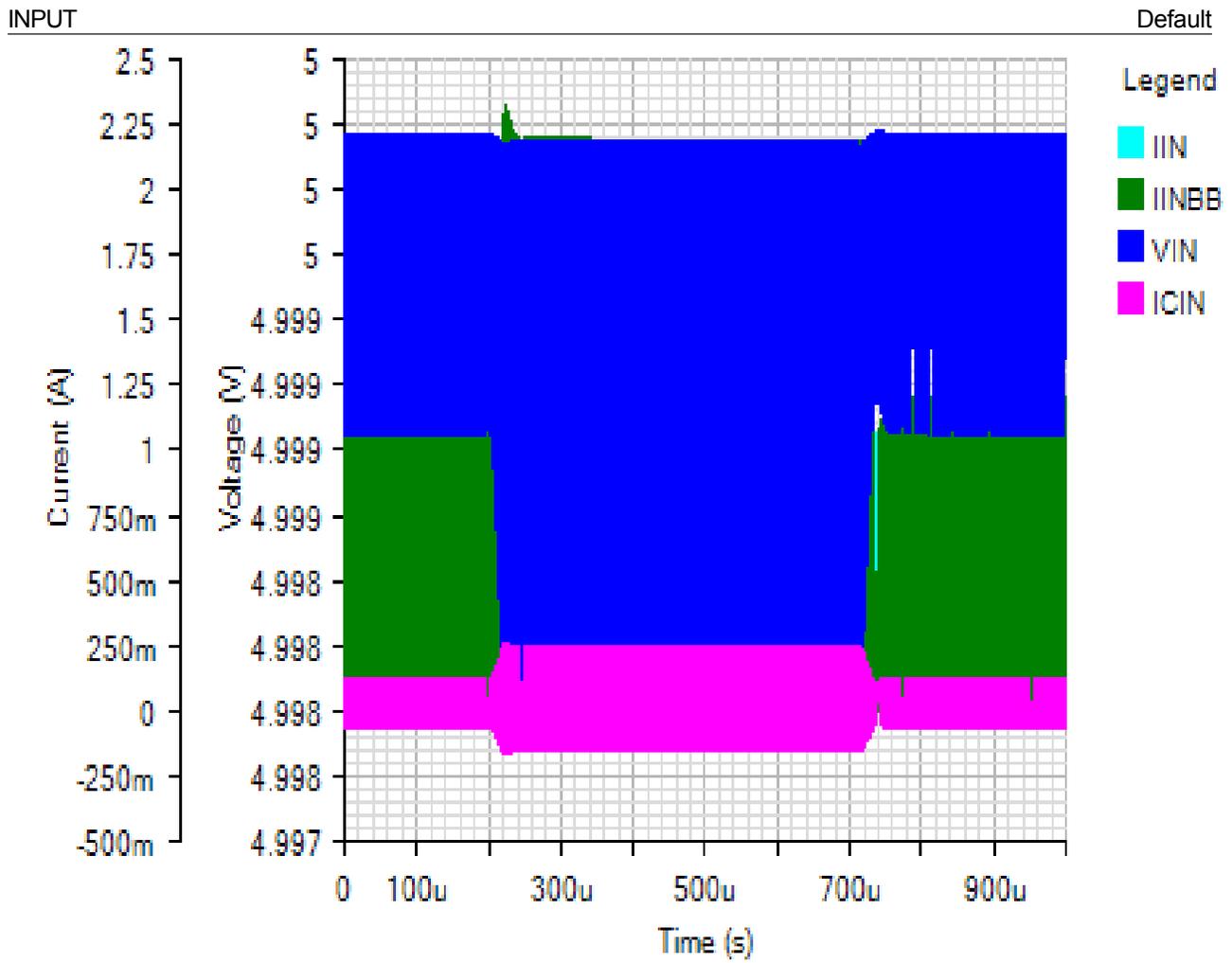


SWITCHING

Default

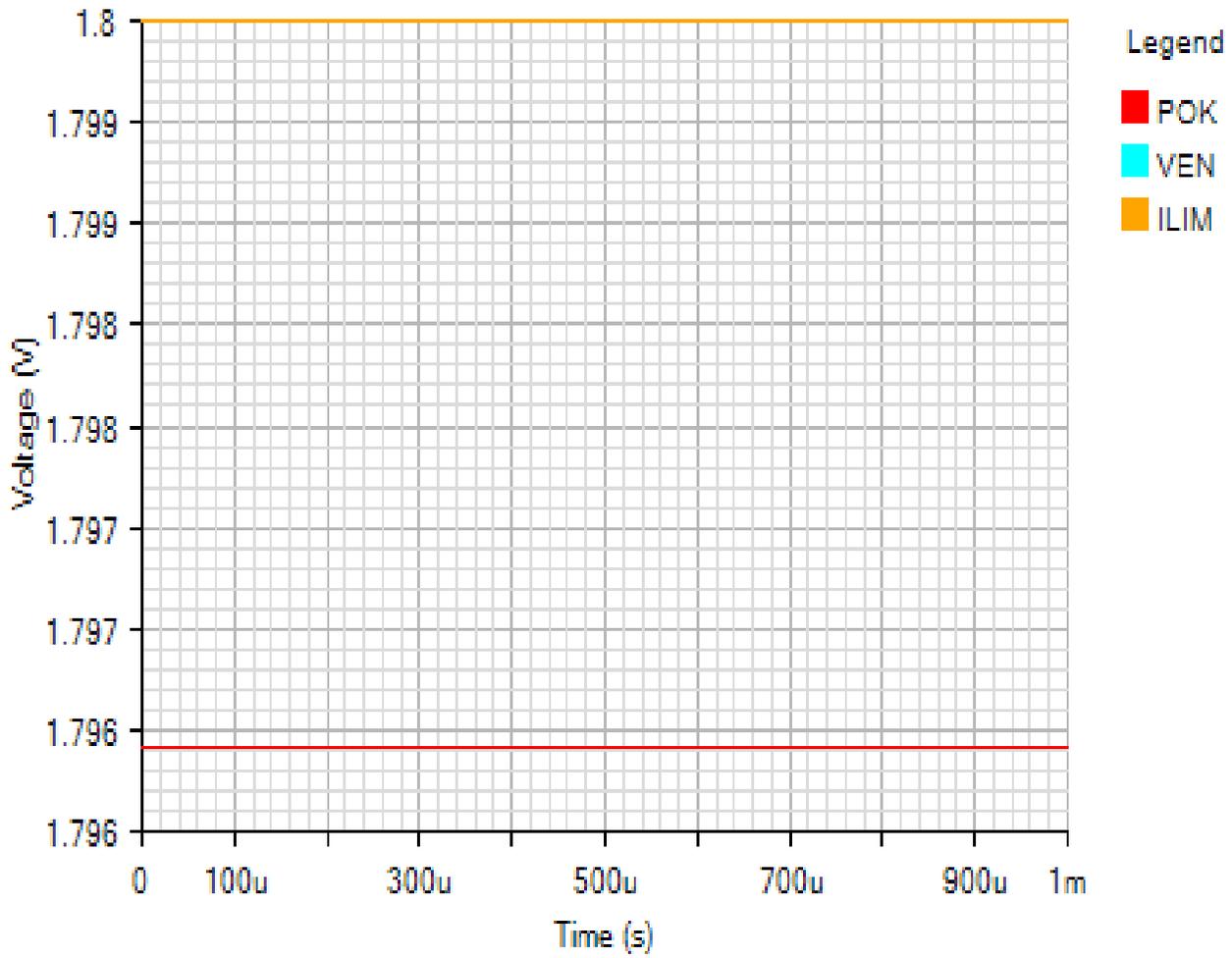


Load Step - Wed Feb 13 2019 09:32:21



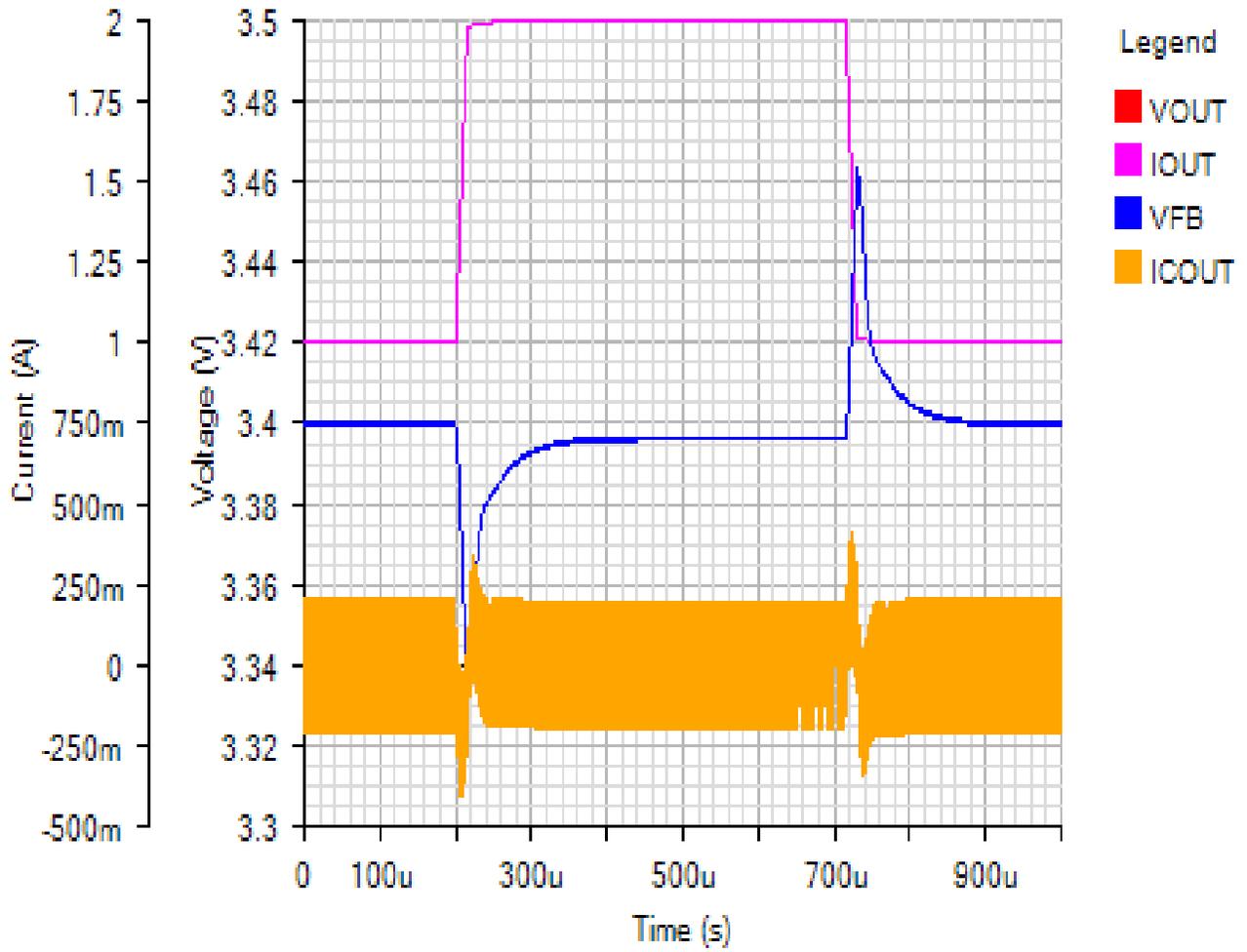
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Default



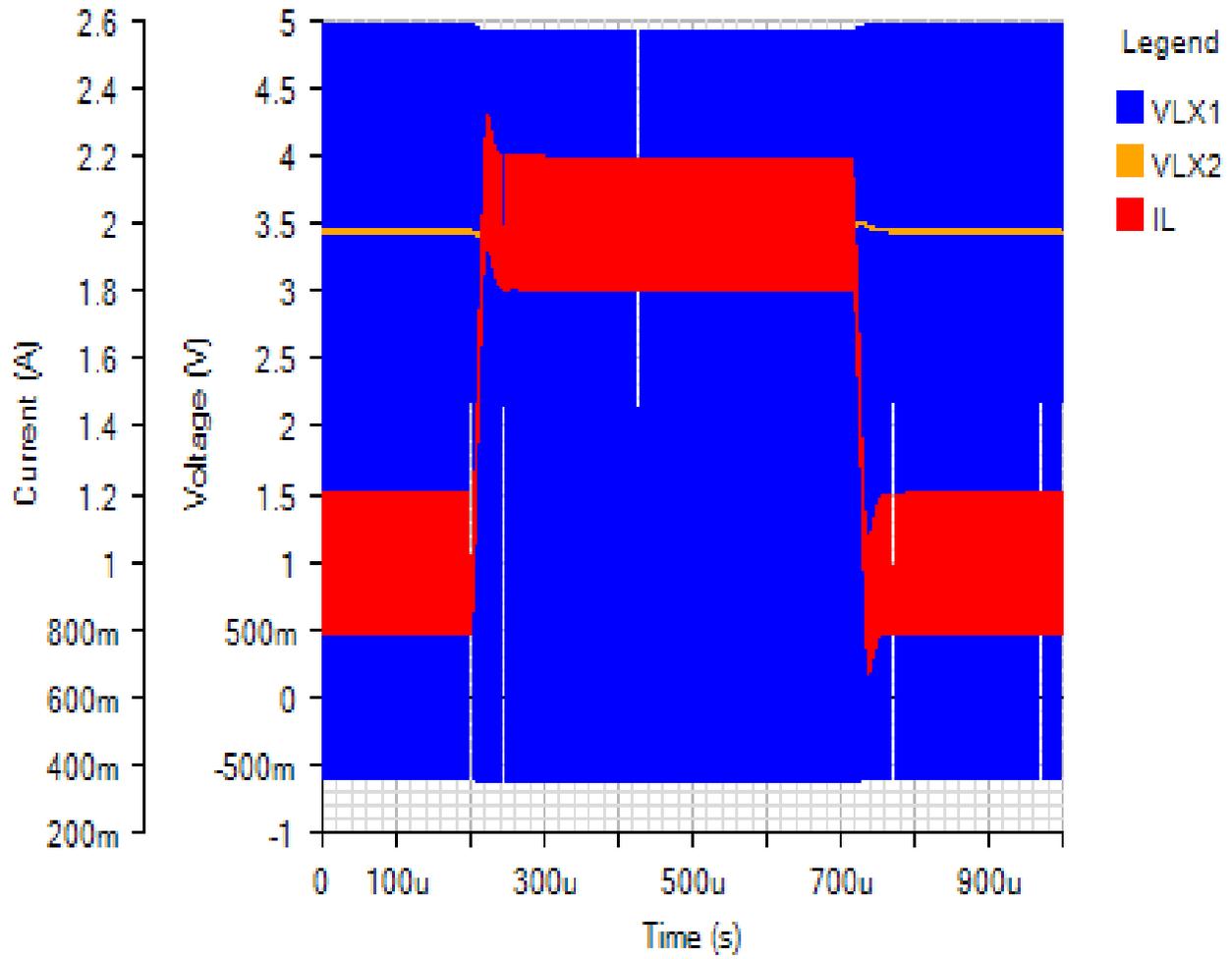
OUTPUT

Default



SWITCHING

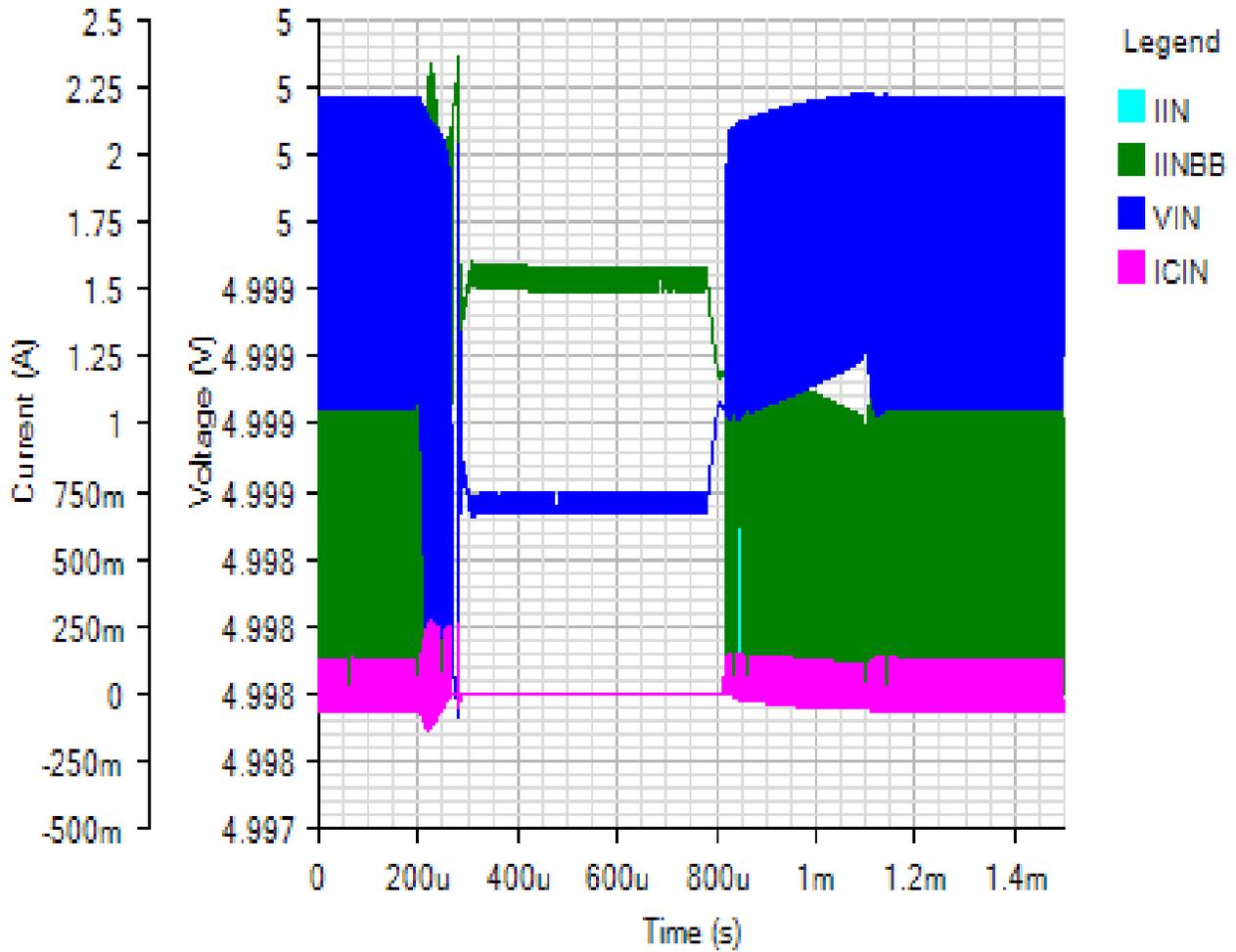
Default



Output Voltage Change - Wed Feb 13 2019 09:32:21

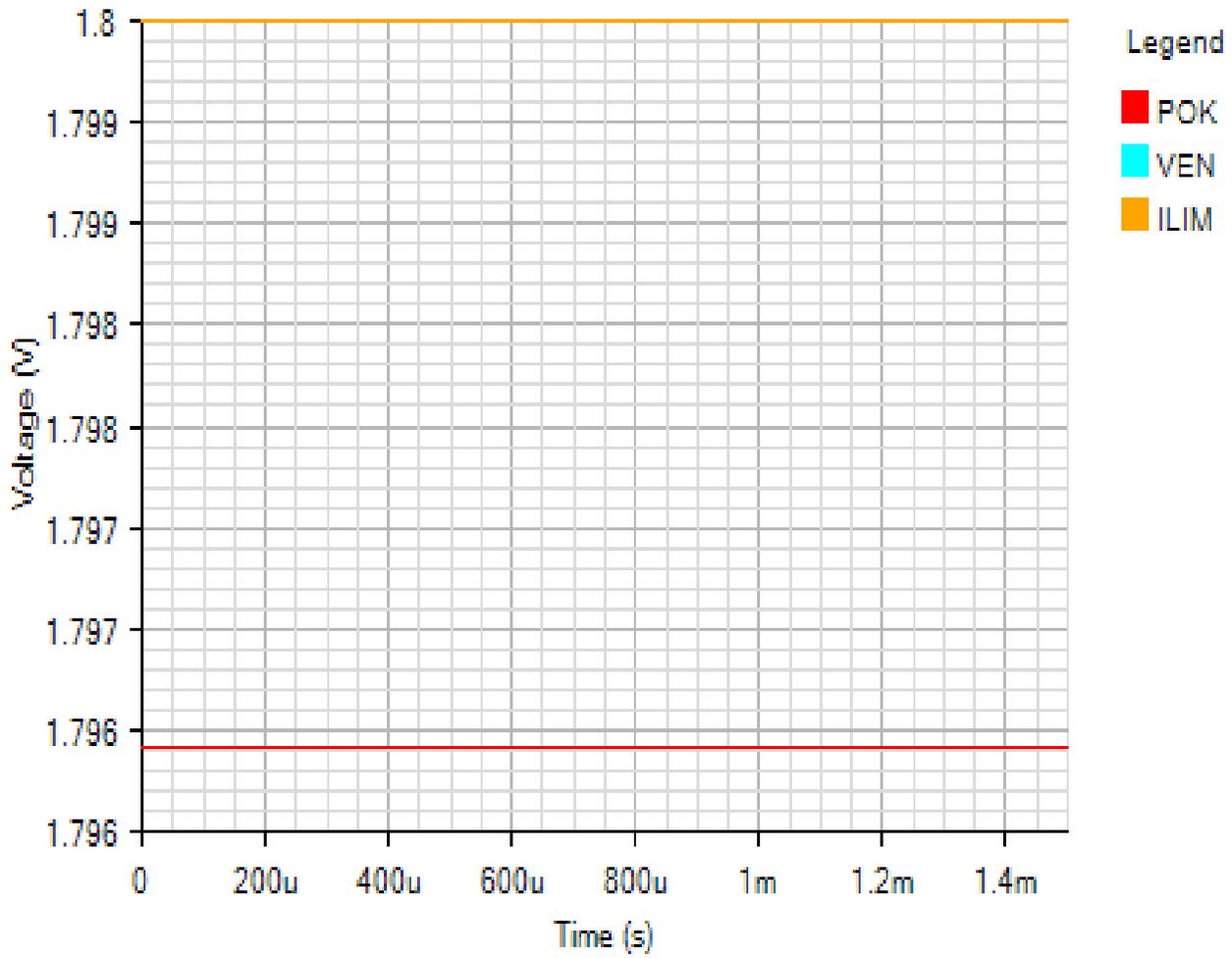
INPUT

Default



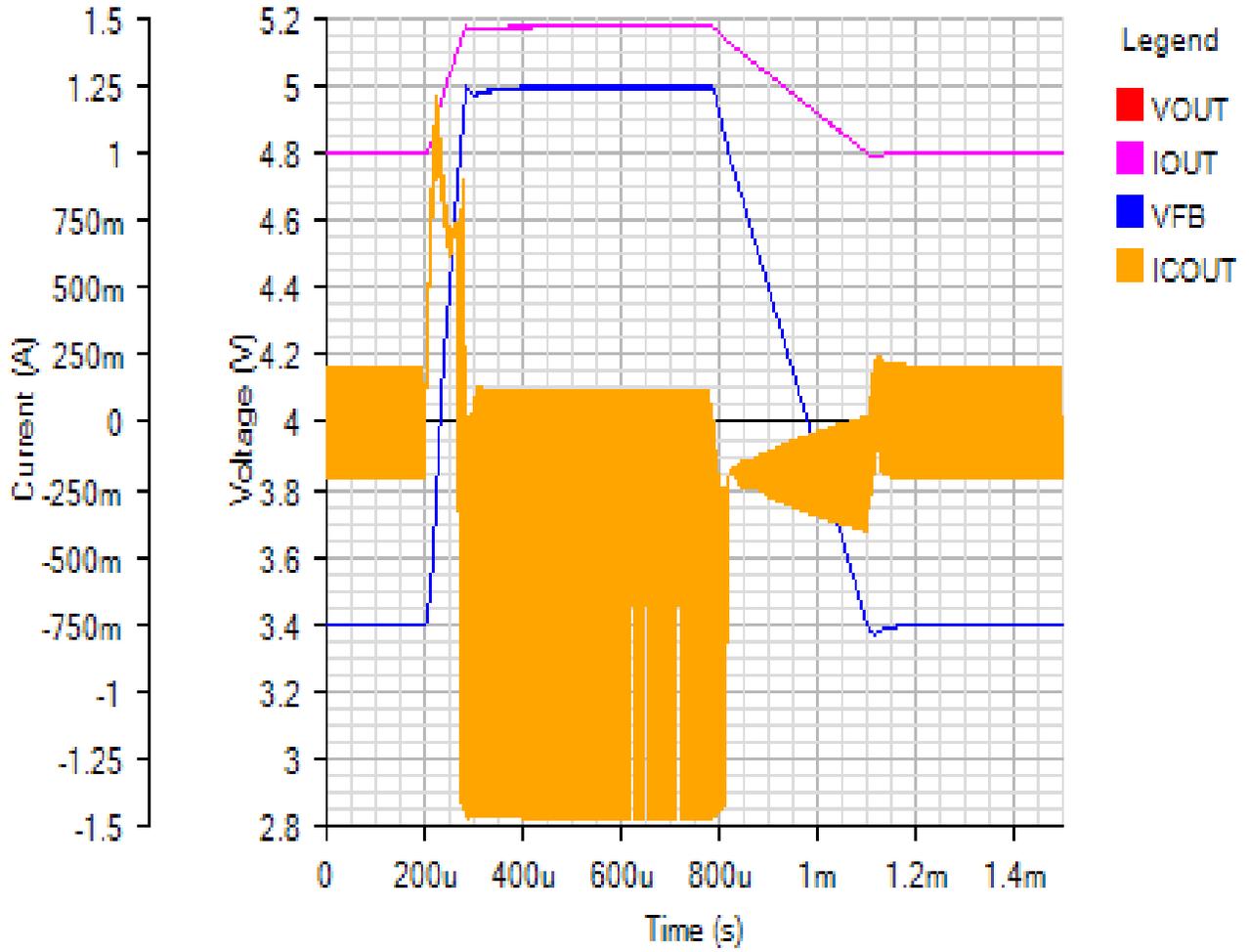
IC

Default



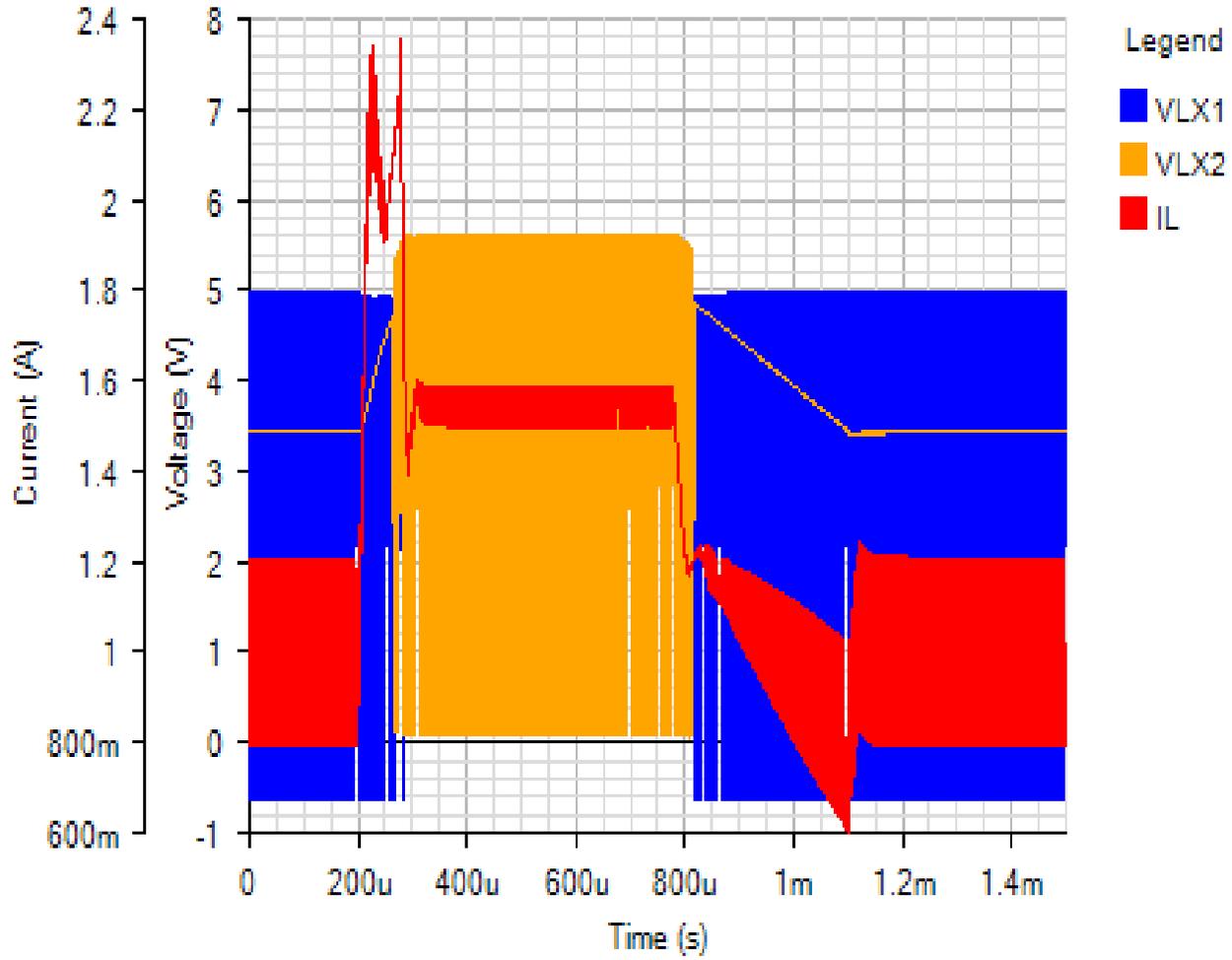
OUTPUT

Default

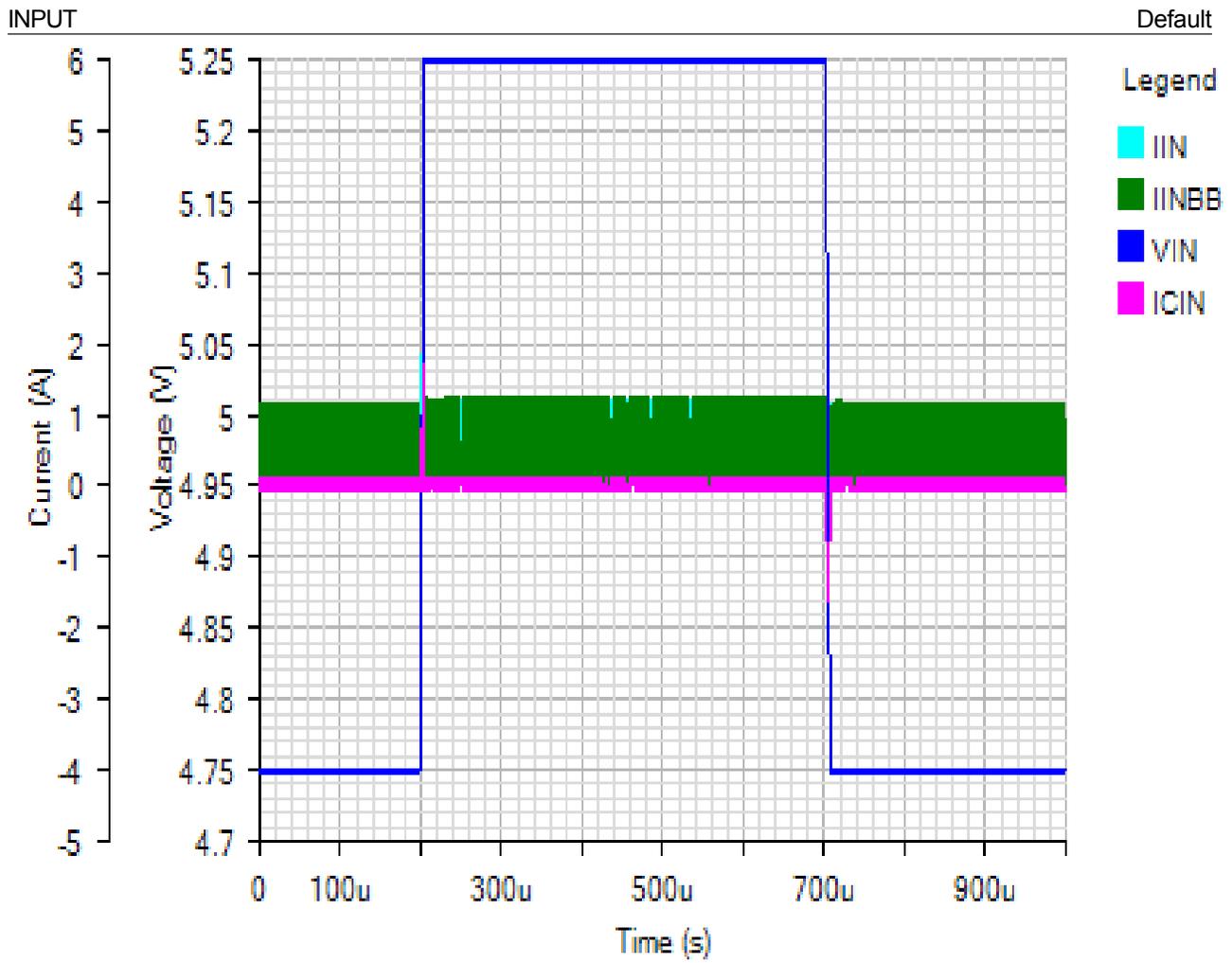


SWITCHING

Default

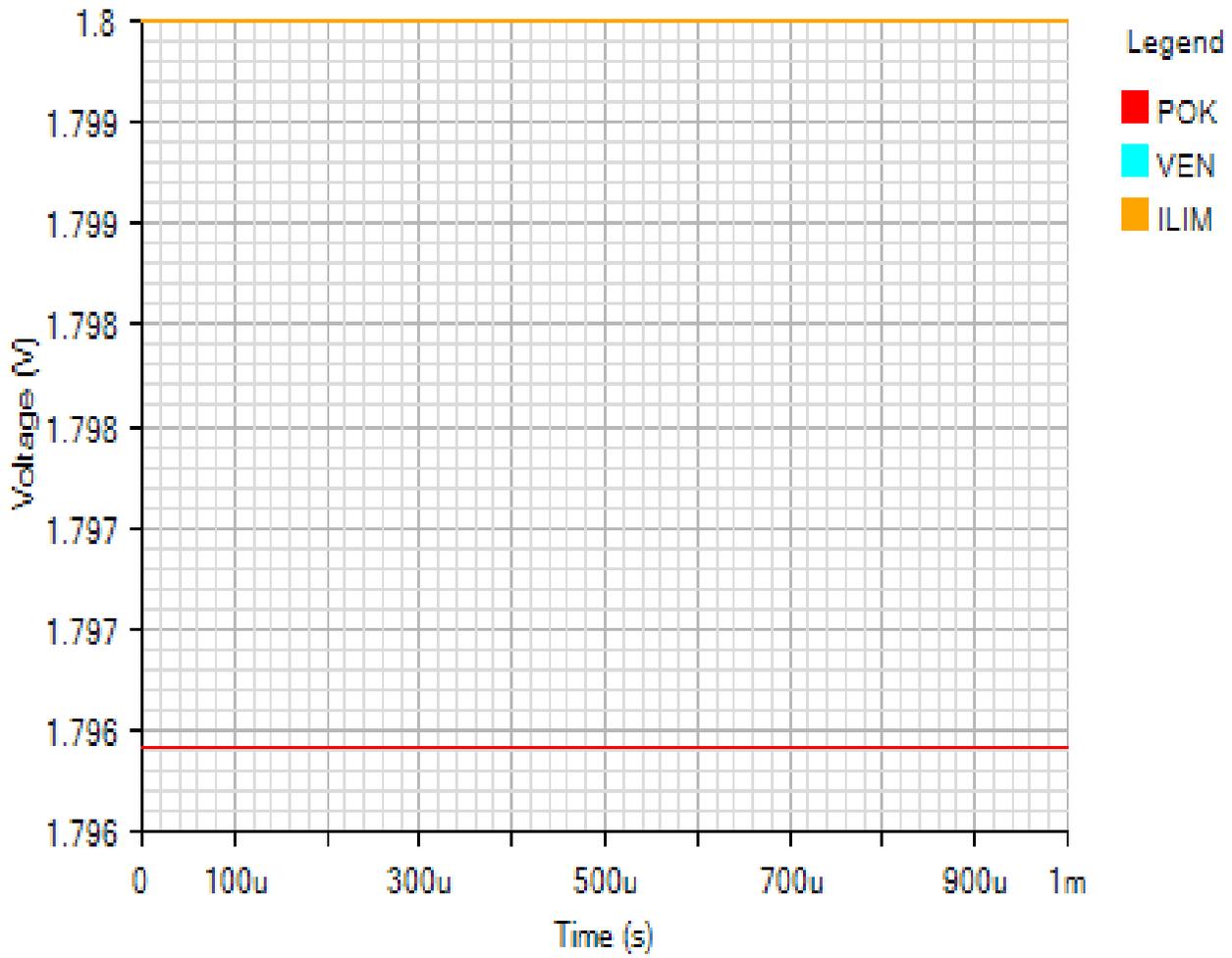


Line Transient - Wed Feb 13 2019 09:32:21



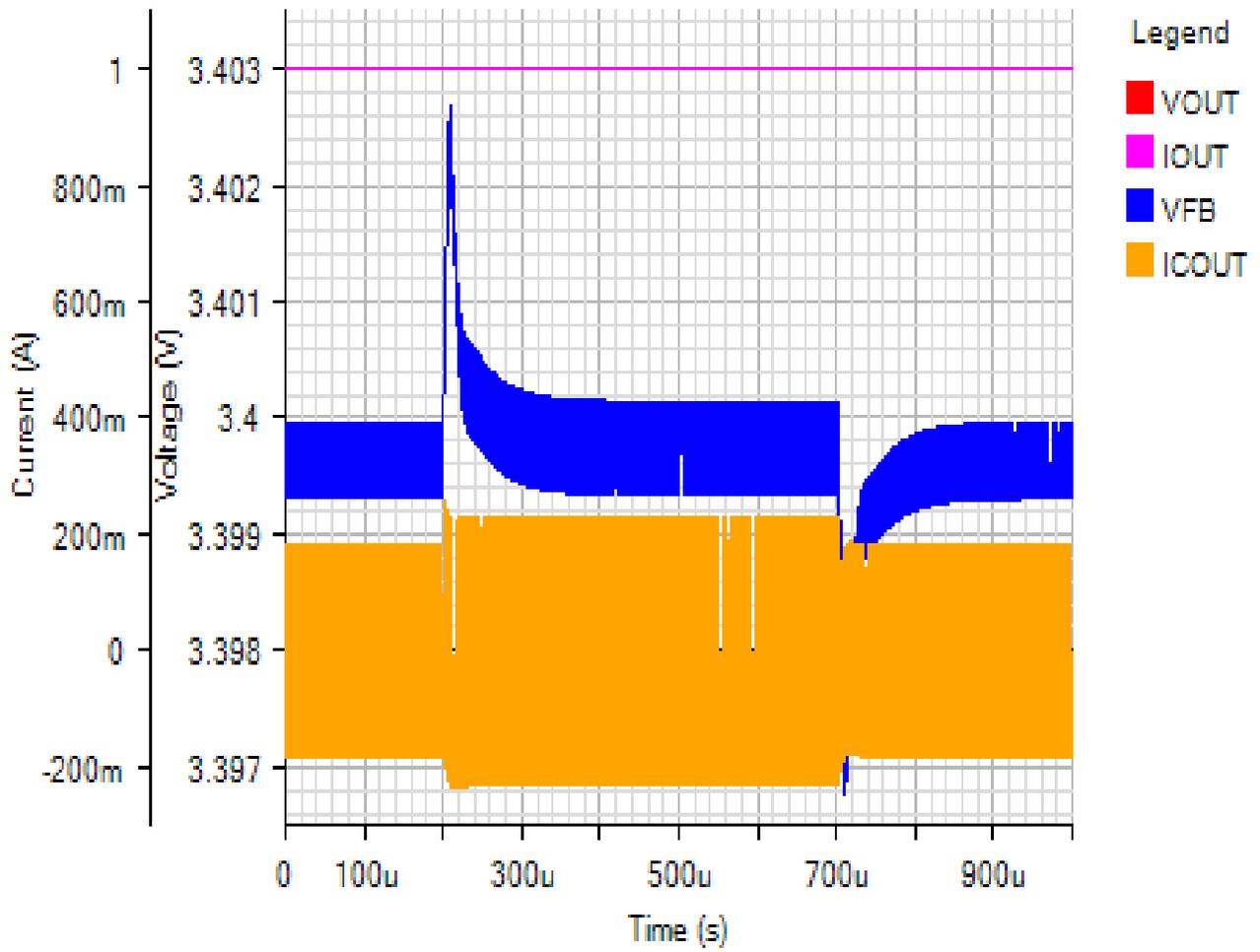
IC

Default



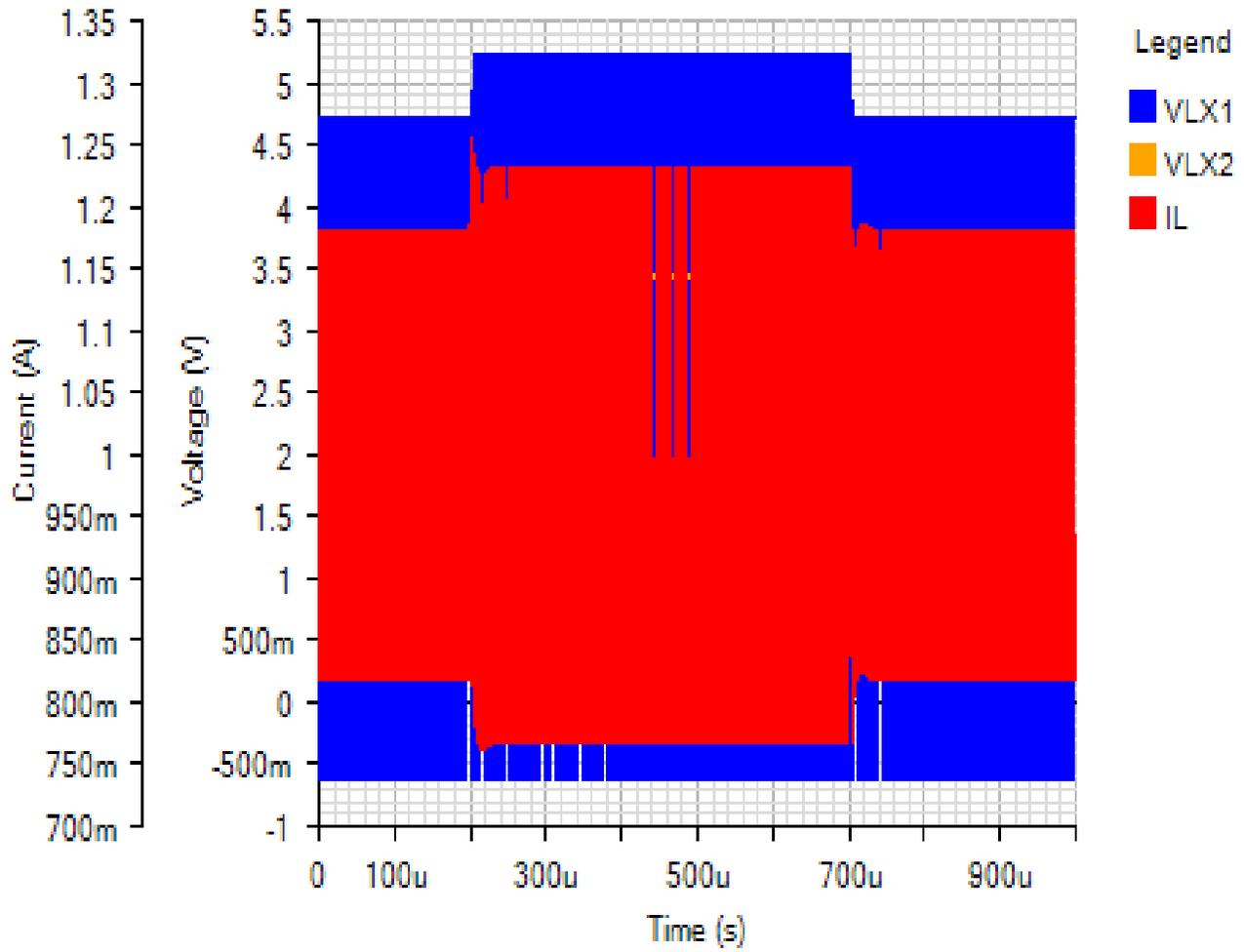
OUTPUT

Default



SWITCHING

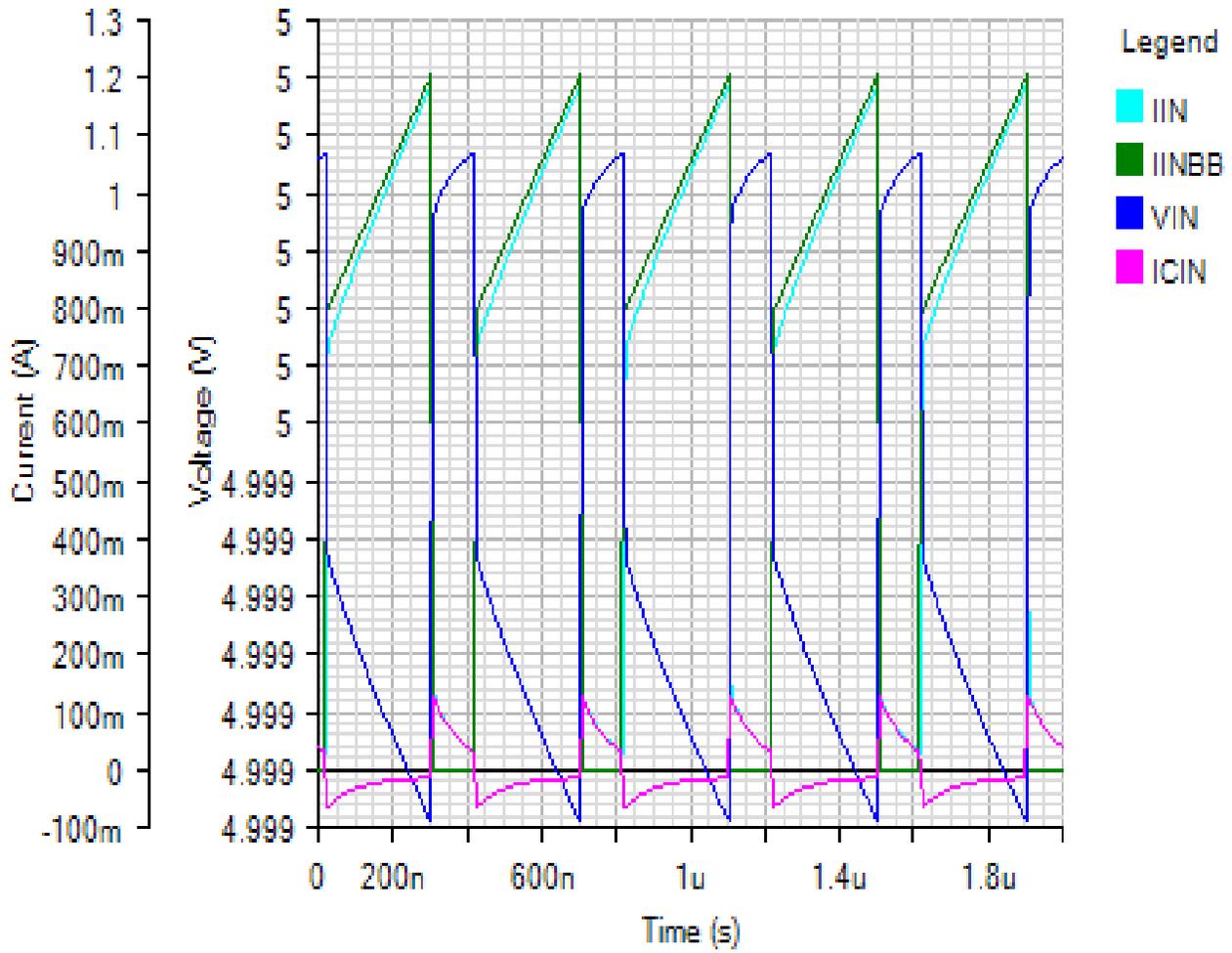
Default



Steady State - Wed Feb 13 2019 09:32:21

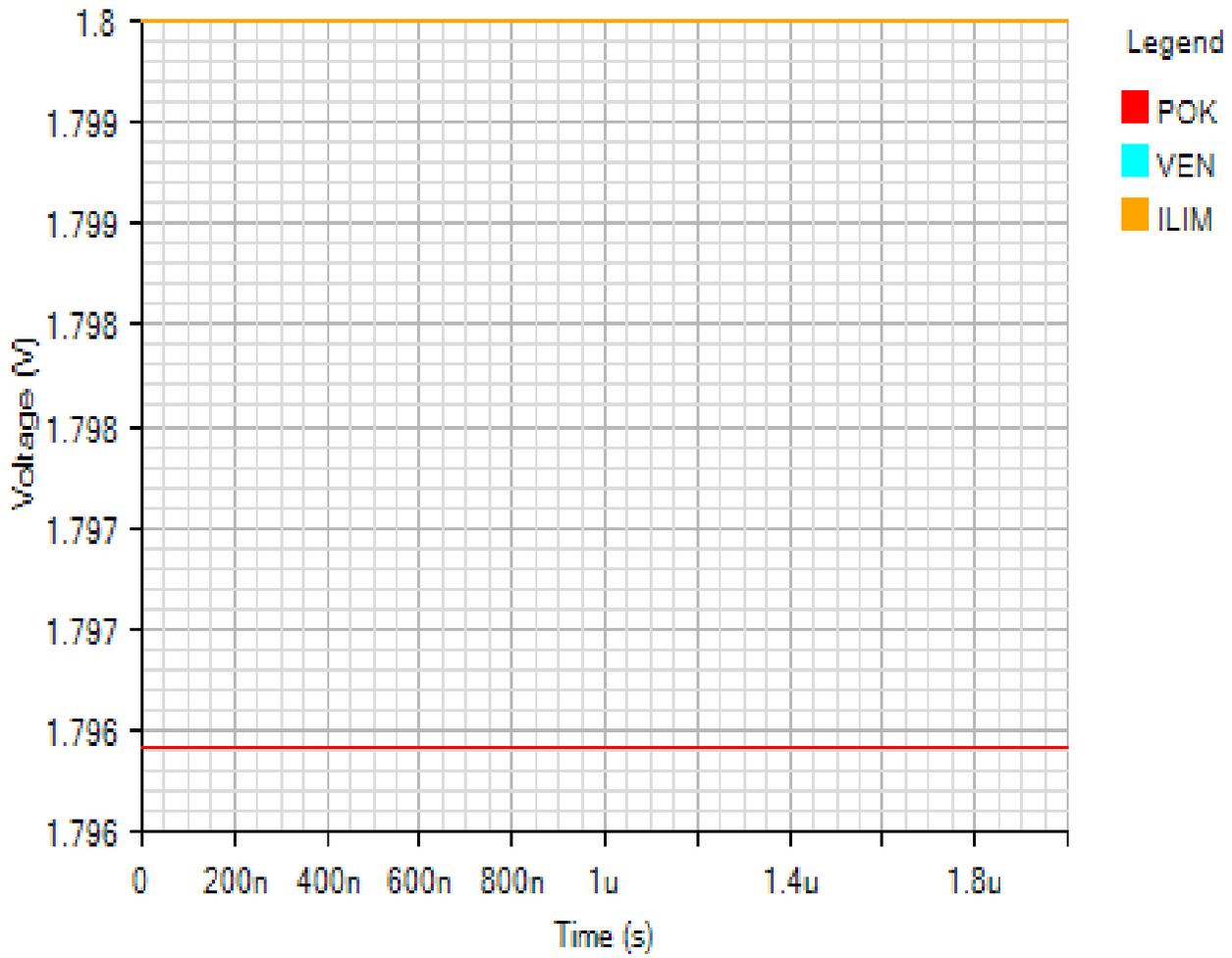
INPUT

Default



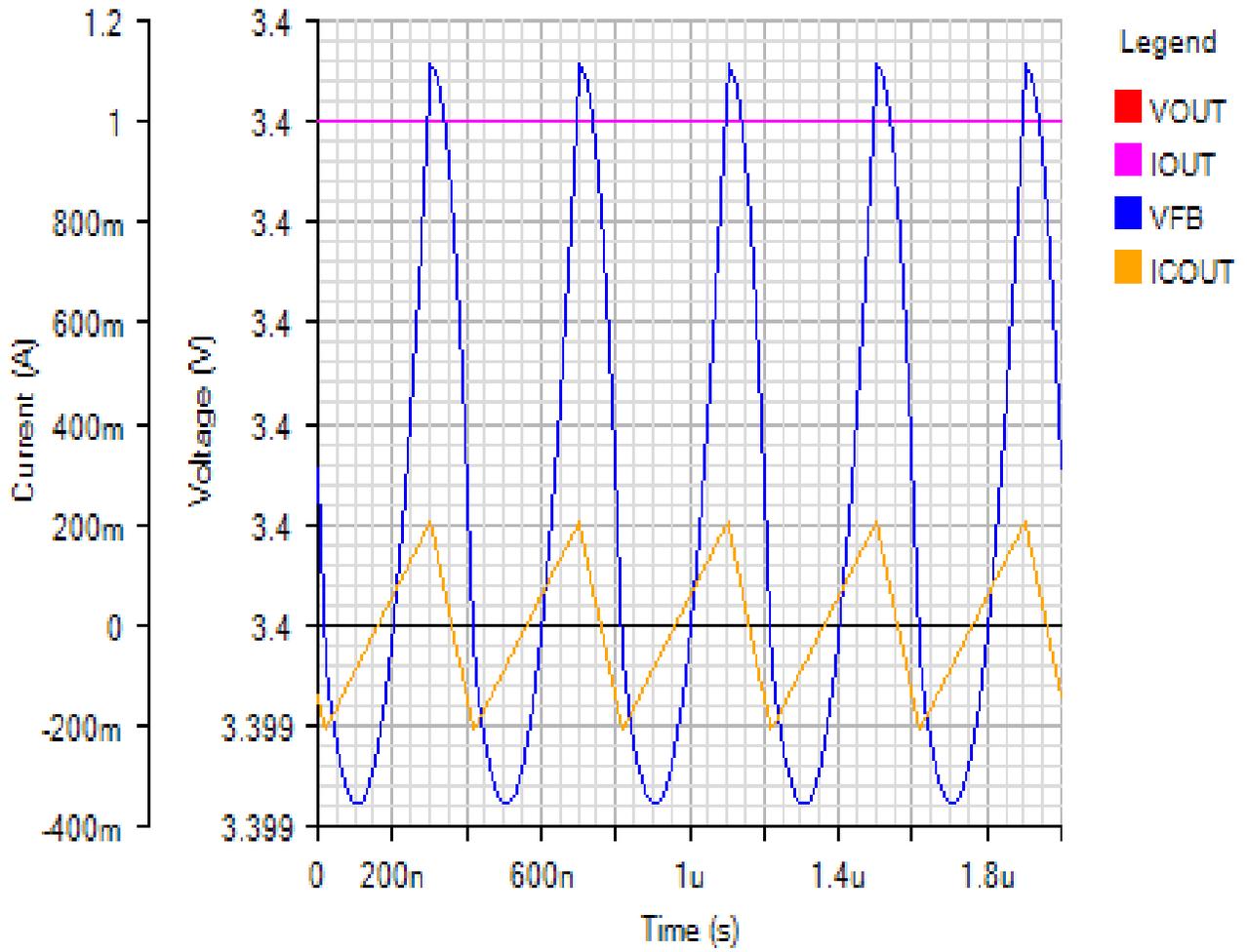
IC

Default



OUTPUT

Default



SWITCHING

Default

