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Fabrication Drawings & Notes

MAX14871 SHIELD BOARD

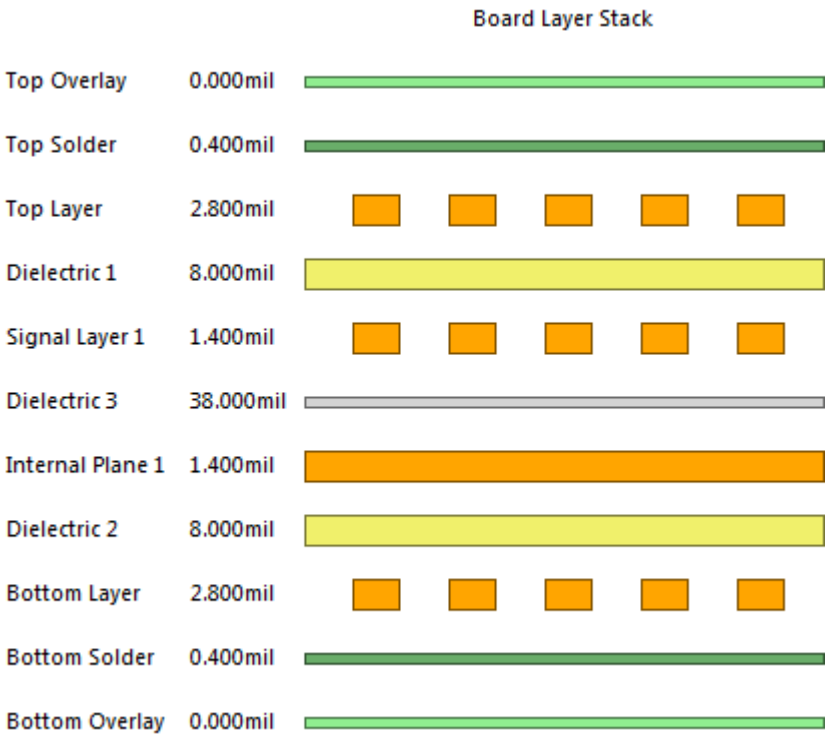
Part Number

MAXREFDES89#

REV A

8/12/2015

Visual Stack-Up



OK TO USE COPPER FOIL CONSTRUCTION

Layer Descriptions

Layer Name	File Extension	Layer Description
Layer #1Top Layer	.GTL	Top Layer
Layer# 2	.G1	GND Plane
Layer# 3	.GP1	Power Plane
Layer# 4	.GBL	Bottom Layer
Top Overlay	.GTO	Top Overlay (Silkscreen)
Bottom Overlay	.GBO	Bottom Overlay (Silkscreen)
Top Pad Master	.GPT	Top Pad Master
Bottom Pad Master	.GPB	Bottom Pad Master
Top Solder Mask	.GTS	Top Solder Mask
Bottom Solder Mask	.GBS	Bottom Solder Mask
Keep-Out Layer	.GKO	Keep-Out Layer
Board Outline	.GM12	Board Outline
Aperture List	.APR	Aperture List
Drill File	.DRL	Drill File (EIA Format)
Drill File	.DRR	Drill File (Tool Sizes)
Drill File	.TXT	Drill File (ASCII Format)
Drill File	.GDD	Drill Drawing
Drill File	.GDG	Drill Guide
Status Report	.REG	Status Report
Layer Report	.REP	Layer Report

Notes: Unless otherwise specified:

1. **Applicable latest corporate specification and documentation:**
   - 1.1 ☒ General Specification for Printed Circuit Fabrication. IPC-A-600, Class 2.
   - 1.2 Part No. _____

2. **Material:**
   - 2.1 ☐ Nema FR-4 Tg> 130c FRP-226 or equivalent, to conform to UL 94V-0.
   - 2.2 ☒ Nema FR-4 High Tg 170c or equivalent.
   - 2.3 ☐ Nema FR-5 Tg> 170c
   - 2.4 ☐ Nema Bt/Epoxy Tg> 185c
   - 2.5 ☐ Nema Polyimide Tg> 220-260c.
   - 2.6 ☐ Other: Specify:

3. **Copper Weight:**
   - 3.1 ☒ **Start Size:**
     - 3.1.1 ☒ External Size:
       - 3.1.1.1 ☐ 1/4 oz. Copper.
       - 3.1.1.2 ☐ ½ oz. Copper.
       - 3.1.1.3 ☒ 1oz. Copper.
       - 3.1.1.4 ☐ 2oz. Copper.
     - 3.1.2 ☒ Internal Size:
       - 3.1.2.1 ☐ ½ oz. Copper.
       - 3.1.2.2 ☒ 1 oz. Copper.
       - 3.1.2.3 ☐ 2 oz. Copper.
   - 3.2 ☒ Finish Size (External Layers Only):
     - 3.2.1 ☐ 1oz. = 1.4 mils
     - 3.2.2 ☐ 1.4oz = 1.9 mils
     - 3.2.3 ☒ 2oz. = 2.8 mils

4. **Drilling:**
   - 4.1 All holes are to be located by the X-Y coordinates from the NC drill data supplied. See legend for finished hole sizes and quantity. P = Plated N = Nonplated.
   - 4.2 ☐ Buried Via's between layers **XX** and **XX.**
   - 4.3 ☐ Other: Specify:

5. **Layer Stack-Up:**
   - 5.1 ☐ Controlled Impedance.
   - 5.2 ☐ Controlled Cross Section.
   - 5.3 ☒ Multi-Layer No. of Layers: **4**
   - 5.4 ☐ 50 Ohms Impedance, = **xx** mil traces.
   - 5.5 ☐ 75 Ohms Impedance, = **xx** mil traces.
   - 5.6 ☐ Coplanar.
   - 5.7 ☐ Differential:
     - 5.7.1 ☐ Edge Coupled.
     - 5.7.2 ☐ Broadside.
   - 5.8 ☐ Other Impedance: Specify:

     _____
   - 5.9 ☒ Please phone and fax customer with any changes on the Controlled Impedance Stack-Up prior to manufacturing.

6. **Stack-Up Sequence:**
   - 6.1 Layer 1, **mal14871 shield.GTL**
     - 6.1.1 Spacing**: 8 MILS**
   - 6.2 Layer 2, **mal14871 shield.G1**
     - 6.2.1 Spacing**: 38 MILS**
   - 6.3 Layer 3, **mal14871 shield.GP1**
     - 6.3.1 Spacing**: 8 MILS**
   - 6.4 Layer 4, **mal14871 shield .GBL**
   - 6.5 ☐ Buried Capacitance between Layers using buried capacitance material.
     - 6.5.1 Between Layer **XX** and **XX**.

7. Plating:

7.1 ☒ Hole wall plating to be > .001" All hole sizes are after plating.
7.2 ☐ Edge connector fingers shall be plated with Nickel/Gold > 15 microinches minimum of gold.
7.3 ☐ Via in pads to be filled with non conductive ink and plated over.
7.4 ☐ Organic coating over copper CU 106A.
7.5 ☒ Immersion Gold, 3-5 micro inches gold over 100 micro inches nickel min.
7.6 ☐ Electroplated Gold, 3-8 micro inches gold over 100-150 micro inches nickel.
7.7 ☐ Bondable gold flash, 6-10 micro inches gold over 175-200 micro inches nickel.
7.8 ☐ Gold Body Flash.
7.9 ☐ Other: Specify:

8. Soldermask:

8.1 Apply solder mask using option specified below:
8.2 ☐ Color = Black.
8.3 ☐ Color = Blue.
8.4 ☒ Color = Green.
8.5 ☐ Color = Red.
8.6 ☐ Color = Other _____
8.7 ☐ Apply solder mask over bare copper.
8.8 ☐ Screen mask PC401 or equivalent.
8.9 ☒ Liquid photo imaginable (LPI). Per IPC-SM-840, Class III.
8.10 ☐ No Solder Mask required.
8.11 ☒ Add barrel relief to vias if needed.
8.12 ☐ Via's plugged.

9. Silkscreen:

9.1 ☐ Component side.
9.2 ☐ Solder side.
9.3 ☒ Both sides.
9.4 ☐ No silkscreen.
9.5 ☒ Use a Non-Conductive epoxy ink, color as marked below:
  9.5.1 ☒ White.
  9.5.2 ☐ Yellow.
  9.5.3 ☐ Black.
  9.5.4 ☐ Other, Specify:
9.6 Vendor markings in silkscreen on bottom side of board:
  9.6.1 ☒ Vendor logo.
  9.6.2 ☒ UL logo.
  9.6.3 ☒ Date code.
  9.6.4 ☐ Primary side.
  9.6.5 ☒ Solder side.
  9.6.6 ☒ Vendor may etch "Date Code".
  9.6.7 ☐ Serial numbering of boards. (Scribing of serial numbers is acceptable, XX-YY" i.e.: XX = panel number, YY = board number.)
  9.6.8 ☒ Domestic vendors only to silkscreen "Made in USA" .

10. Dimensions:

10.1 ☒ All dimensions are in inches; hole sizes are in mils.
10.2 ☐ All dimensions are in millimeters; hole sizes are in mm.
10.3 ☐ Other, Specify:

11. Annular Ring:

11.1 ☒ .002 min. on external layers.
11.2 ☒ .001 min. on internal layers.
11.3 ☒ Via's tangency is ok
11.4 ☐ Does Not Apply.
11.5 ☐ Other, Specify:

12. Thieving:

12.1 ☐ It is ok to apply Thieving .030" Squares on .050" Centers and .100" away from features.

12.2 ☐ Do NOT Apply Thieving

13. **Tolerances:**

13.1 ☒ Unless marked otherwise on fab drawing finished hole tolerance: +/- .003 **(See attached fabrication and drill drawings for plated and non-plated holes)**

13.2 ☐ Angle tolerance: +/- 2 deg.

13.3 ☒ Dielectric thickness:

13.3.1 .003 - .010 (+/- .001)

13.3.2 .011 - .015 (+/- .0015)

13.3.3 .016 - .028 (+/- .002)

13.3.4 .029 - .038 (+/- .003)

13.3.5 .039 – Up (+/- .004)

13.4 ☒ No conductor width to be less than given dimension of**: 10 mils**

13.5 ☒ Nick or holes shall not reduce trace width by more then: **10%.**

13.6 ☒ Registration of holes shall be within true position, +/- .003

13.7 ☒ Overall board finished thickness to be**: 62 mils** +/- 10%

13.9 ☒ Fabricated board must be flat within .010" across a 6" span. As per IPC-A-6

14. Layer Stripping:

14.1 ☒ No Stripping.

14.2 ☐ Stripes of copper are plotted on each layer along the edge shown. These "Stacking" strips are intended to be exposed when the PCB is routed from panel

15. Testing:

15.1 ☒ PCB shall be electrically tested to CAD/Gerber net list provided.

15.2 ☒ Compare CAD/Gerber net list to Gerber net list prior to fabricating PCB. Fabricate only if lists agree.

15.3 ☒ Check for violations from pad to pad, trace to pad, trace to trace etc. Minimum clearances to be: 6 **mils.**

15.4 ☐ Test for Impedance of: **50** Ohms.

15.5 ☐ Test for Impedance of: **75** Ohms.

15.6 ☐ Test for impedance of: _____

15.7 ☐ TDR coupon ship with boards

15.8 ☐ Include Controlled Impedance Stack-Up Form Report with finish board

16. Panels:

16.1 ☒ Route boards around entire outline.

16.2 ☐ Route boards with breakout tabs.

16.3 ☐ V Grove Scoring.

16.4 ☐ Other, Specify: _____

17. Solder Samples

17.1 ☒ Provide 1 ea. Solder Sample.

17.2 ☐ Do **Not** provide Solder Sample.

18. Compliance Reports

18.1 ☒ Provide all reports in a 4 ¼" x 11" envelope.

☐ Provide all reports in a 10" x 13" envelope