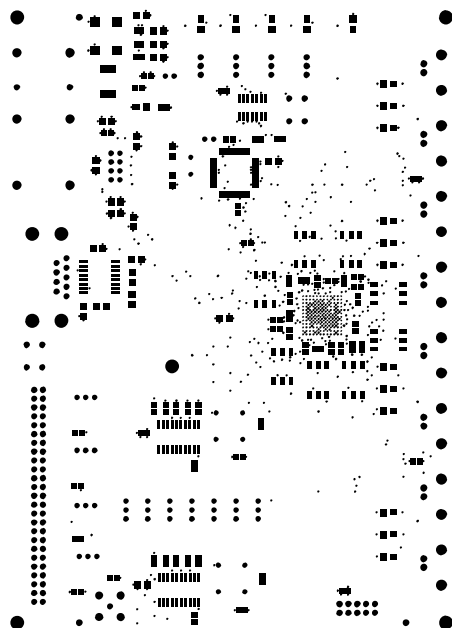
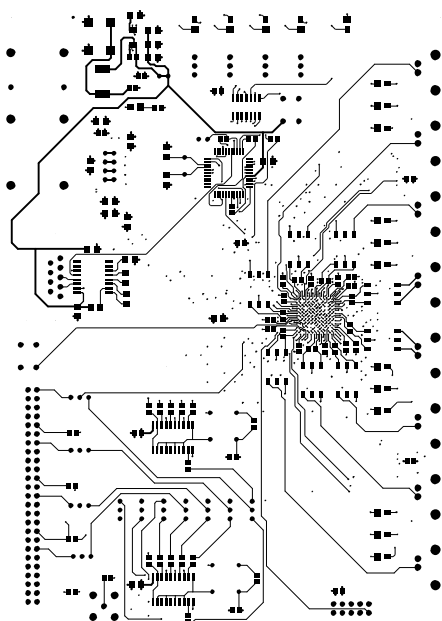


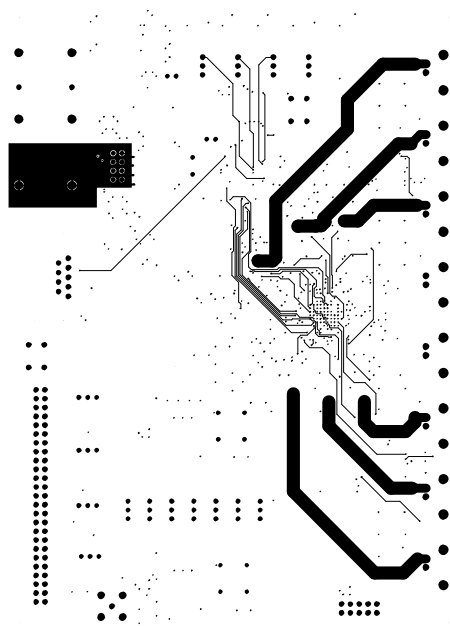
DALLAS SEMICONDUCTOR 2004
DS3254DK01A0
TOP SILKSCREEN



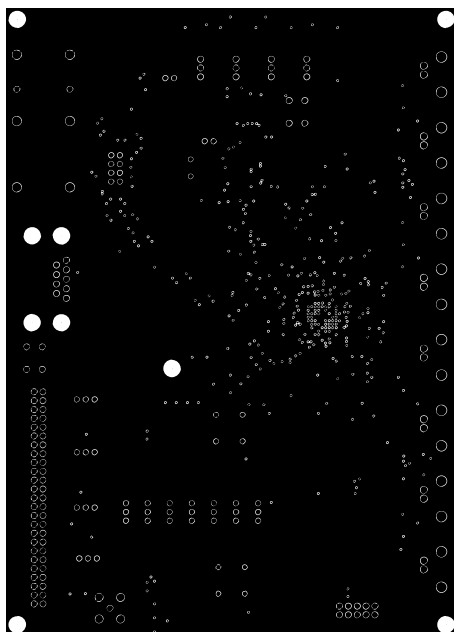
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TOP SOLDERMASK



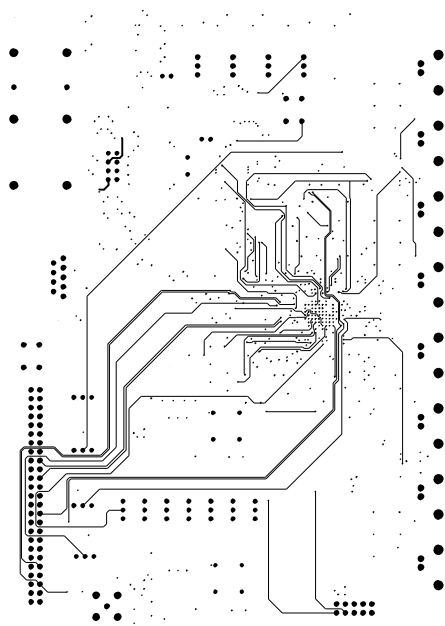
DALLAS SEMICONDUCTOR 2004
DS3254DK01A0
TOP LAYER - SIGNAL



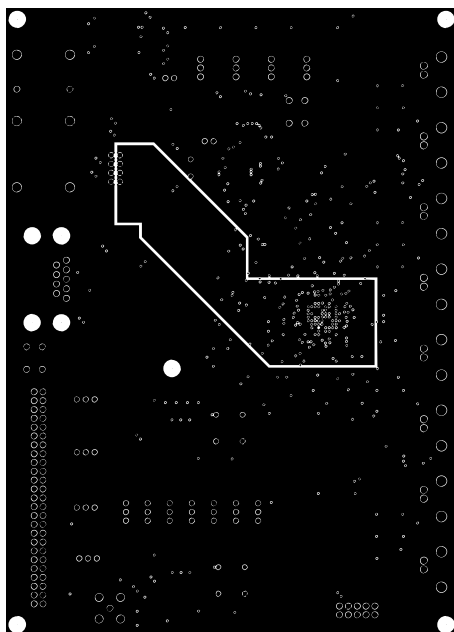
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LAYER 2 SIGNAL



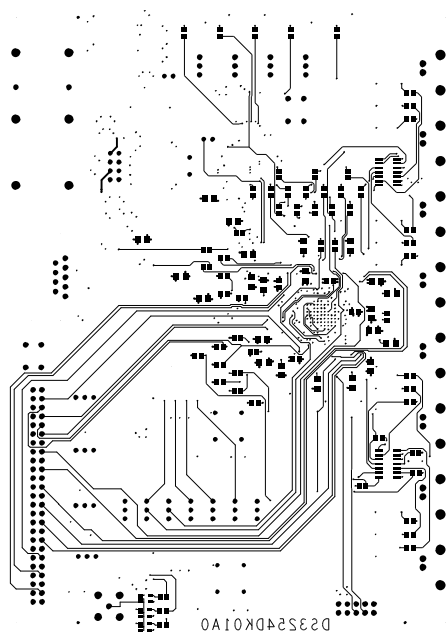
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LAYER 3 GND



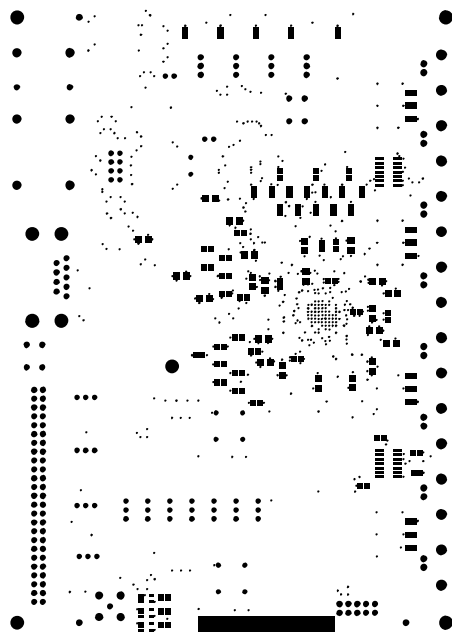
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LAYER 4 SIGNAL



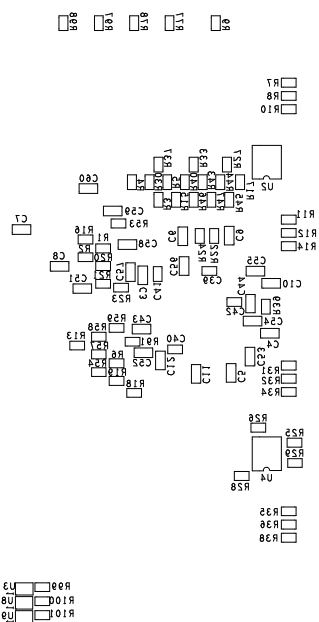
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LAYER 5 V3.3/VDD



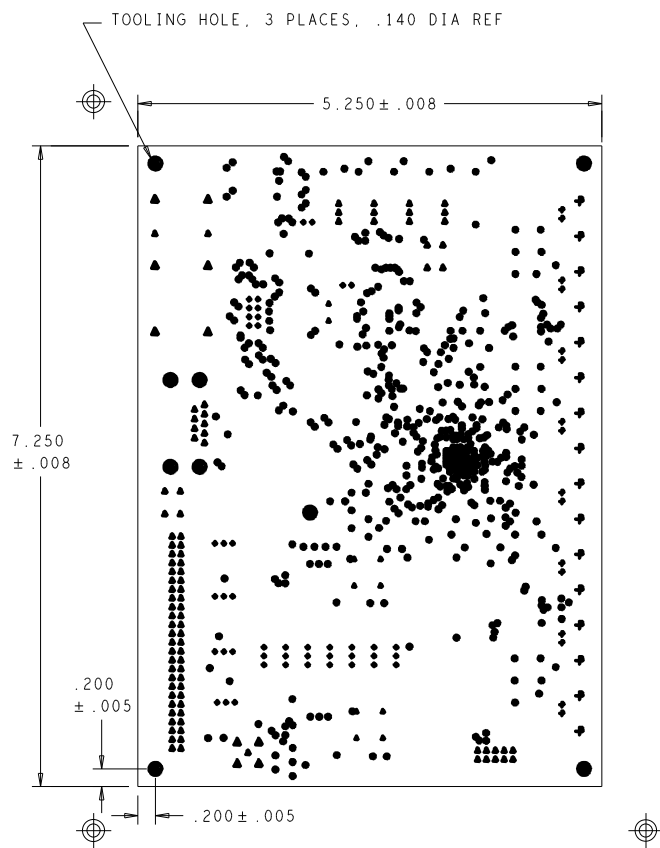
DALLAS SEMICONDUCTOR 2004
DS3254DK01A0
BOTTOM LAYER SIGNAL



DALLAS SEMICONDUCTOR 2004
DS3254DK01A0
BOTTOM SOLDERMASK



DALLAS SEMICONDUCTOR 2004
DS3254DK01A0
BOTTOM SILKSCREEN



DALLAS SEMICONDUCTOR 2004
DS3254DK01A0
FABRICATION DRAWING

DRILL CHART				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	+/- TOL	PLATED	QTY
●	10.0	+0/-10	PLATED	545
▲	36.0	3.0	PLATED	10
•	40.0	3.0	PLATED	45
▲	48.0	3.0	PLATED	92
◆	50.0	3.0	PLATED	16
▲	71.0	3.0	PLATED	4
◆	85.0	3.0	PLATED	16
▲	85.0	3.0	PLATED	6
●	140.0	3.0	NON-PLATED	9

LAYER 1 - TOP.ART (1/2 OZ)
LAYER 2 - L2.ART (1/2 OZ)
LAYER 3 - L3.ART (1/2 OZ)
LAYER 4 - L4.ART (1/2 OZ)
LAYER 5 - L5.ART (1/2 OZ)
LAYER 6 - BOTTOM.ART (1/2 OZ)

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL - FR4, DIELECTRIC CONSTANT 4.1.
2. THICKNESS: .079 +/- 10% AFTER PLATING.
3. BUILD/MANUFACTURE TO BEST COMMERCIAL STANDARDS.
4. HOLE SIZES ARE FINISHED SIZE.
5. MINIMUM CONDUCTOR WIDTH: .005.
6. MINIMUM CONDUCTOR SPACING: .005.
7. SOLDERMASK: LPI BOTH SIDES WITH EXPOSED SOLDER AREAS SOLDER COATED (63/37 TIN LEAD) AND LEVELED.
8. SILKSCREEN TOP AND BOTTOM SIDES USING WHITE NON-CONDUCTIVE INK.
9. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.
10. COPPER EXTERNAL: 1/2 OZ PLATED UP TO 1 OZ.
11. THE METAL SURFACES OF THE VIAS UNDERNEATH THE BGA ARE TO BE COVERED WITH SOLDER MASK. THOSE VIAS ARE NOT TO BE COMPLETELY TENTED.
12. CONTROLLED IMPEDANCES OF 75 AND 100 OHMS ARE REQUIRED ON VARIOUS NETS IN THE DESIGN. THE FOLLOWING CONDUCTOR LAYER SEPARATIONS ARE REQUIRED:
TOP LAYER TO L2 - .018
TOP LAYER TO L3 - .022
L4 TO L3 - .012
L4 TO L5 - .016
L5 TO L6 - .022