Design Name M:/PCB_LAYOUT/LAYOUT_WORK/Aleksandar_Bjeletic_Saavedra/max20800_d0_apps_d/worklib/max20800_d0_apps_d/physical/max20800_d0_apps_d.brd
Date Tue Mar 27 15:04:40 2018

DRC Error Count Summary

DRC Error Type	DRC Error Count
Package to Package	2
Total DRC Errors	2

Detailed DRC Errors

Constraint Name	DRC Marker Location	Required Value	Actual Value	Constraint Source	Constraint Source Type	Element 1	Element 2	Comment
Package to Package Spacing	(236.20 36.20)	0 MIL	0 MIL	PACKAGE_HEIGHT_MIN	DESIGN	Shape "Mtg2 Package Geometry/Place_Bound_Top"	Shape "Out- Package Geometry/Place_Bound_Top"	Checked and Cleared to fab
Package to Package Spacing	(3700.80 36.20)	0 MIL	0 MIL	PACKAGE_HEIGHT_MIN	DESIGN	Shape "Mtg1 Package Geometry/Place_Bound_Top"	Shape "Out+ Package Geometry/Place_Bound_Top"	Checked and Cleared to fab