Miniature, Low-Profile, 5V/1.5A, Synchronous, No-Opto Flyback DC-DC Converter with 87% Efficiency Using MAX17690 and MAX17606

MAXREFDES1226

Introduction

Due to its simplicity and low cost, the flyback converter is the preferred choice for low-to-medium isolated DC-DC power-conversion applications. However, the use of an optocoupler or an auxiliary winding on the flyback transformer for voltage feedback across the isolation barrier increases the number of components and design complexity. The MAX17690 eliminates the need for an optocoupler or auxiliary transformer winding and achieves ±5% output voltage regulation over line, load, and temperature variations.

The MAX17690 implements an innovative algorithm to accurately determine the output voltage by sensing the reflected voltage across the primary winding during the flyback time interval. By sampling and regulating this reflected voltage when the secondary current is close to zero, the effects of secondary-side DC losses in the transformer winding, the PCB tracks, and the rectifying diode on output voltage regulation can be minimized.

The MAX17690 also compensates for the negative temperature coefficient of the rectifying diode.

Other features include the following:

- 4.5V to 60V Input Voltage Range
- Programmable Switching Frequency from 50kHz to 250kHz
- Programmable Input Enable/UVLO Feature
- Programmable Input Overvoltage Protection
- Adjustable Soft-Start
- 2A/4A Peak Source/Sink Gate Drive Capability
- Hiccup Mode Short-Circuit Protection
- Fast Cycle-by-Cycle Peak Current Limit
- Thermal Shutdown Protection
- Space-Saving, 16-Pin, 3mm x 3mm TQFN Package
- -40°C to +125°C Operating Temperature Range

Hardware Specification

An isolated no-opto flyback DC-DC converter using the MAX17690 and MAX17606 is demonstrated for a 5V DC output application. The power supply delivers up to 1.5A at 5V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	17V	36V
Frequency	f_{SW}	128kHz	
Peak Efficiency at Full Load	η_{MAX}	87%	
Efficiency at Minimum Load	η_{MIN}	60%	
Output Voltage	V_{OUT}	5V	
Output Voltage Ripple	ΔV_O	50mV	
Maximum Output Current	I_{OUT}	1.5A	
Maximum Output Power	P_{OUT}	7.5W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing an isolated no-opto flyback DC-DC converter using Maxim's MAX17690 controller. The power supply has been built and tested.

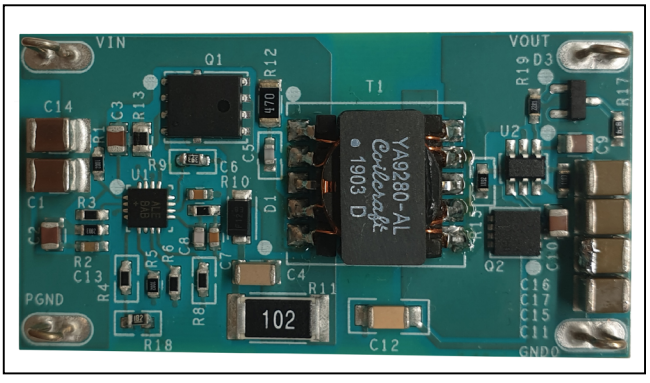

Figure 1. MAXREFDES1226 hardware.

The Isolated No-Opto Flyback Converter

One of the drawbacks encountered in most isolated DC-DC converter topologies is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated back to the primary side to maintain output voltage regulation. In a regular isolated flyback converter, this is normally achieved using an optocoupler feedback circuit or an additional auxiliary winding on the flyback transformer. Optocoupler feedback circuits reduce overall power-supply efficiency, and the extra components increase the cost and physical size of the power supply. In addition, optocoupler feedback circuits are difficult to design reliably due to their limited bandwidth, nonlinearity, high current transfer ratio (CTR) variation, and aging effects. Feedback circuits employing auxiliary transformer windings also exhibit deficiencies. Using an extra winding adds to the flyback transformer's complexity, physical size, and cost, while load regulation and dynamic response are often poor.

The MAX17690 is a peak current-mode controller designed specifically to eliminate the need for optocoupler or auxiliary transformer winding feedback in the traditional isolated flyback topology, therefore reducing size, cost, and design complexity. It derives information about the isolated output voltage by examining the voltage on the primary-side winding of the flyback transformer.

Other than this uniquely innovative method for regulating the output voltage, the no-opto isolated flyback converter using the MAX17690 follows the same general design process as a traditional flyback converter. To understand the operation and benefits of the no-opto flyback converter, it is useful to review the schematic and typical waveforms of the traditional flyback converter (using the MAX17595) shown in Figure 2.

The simplified schematic in Figure 2 illustrates how information about the output voltage is obtained across the isolation barrier in traditional isolated flyback converters. The optocoupler feedback mechanism requires at least 10 components, including an optocoupler and a shunt regulator, in addition to a primary-side bias voltage (V_{BIAS}) to drive the phototransistor. The error voltage (FB2) connects to the FB pin of the flyback controller.

The transformer feedback method requires an additional winding on the primary side of the flyback transformer, a diode, a capacitor, and two resistors to generate a voltage proportional to the output voltage. This voltage is compared to an internal reference in a traditional flyback controller to generate the error voltage.

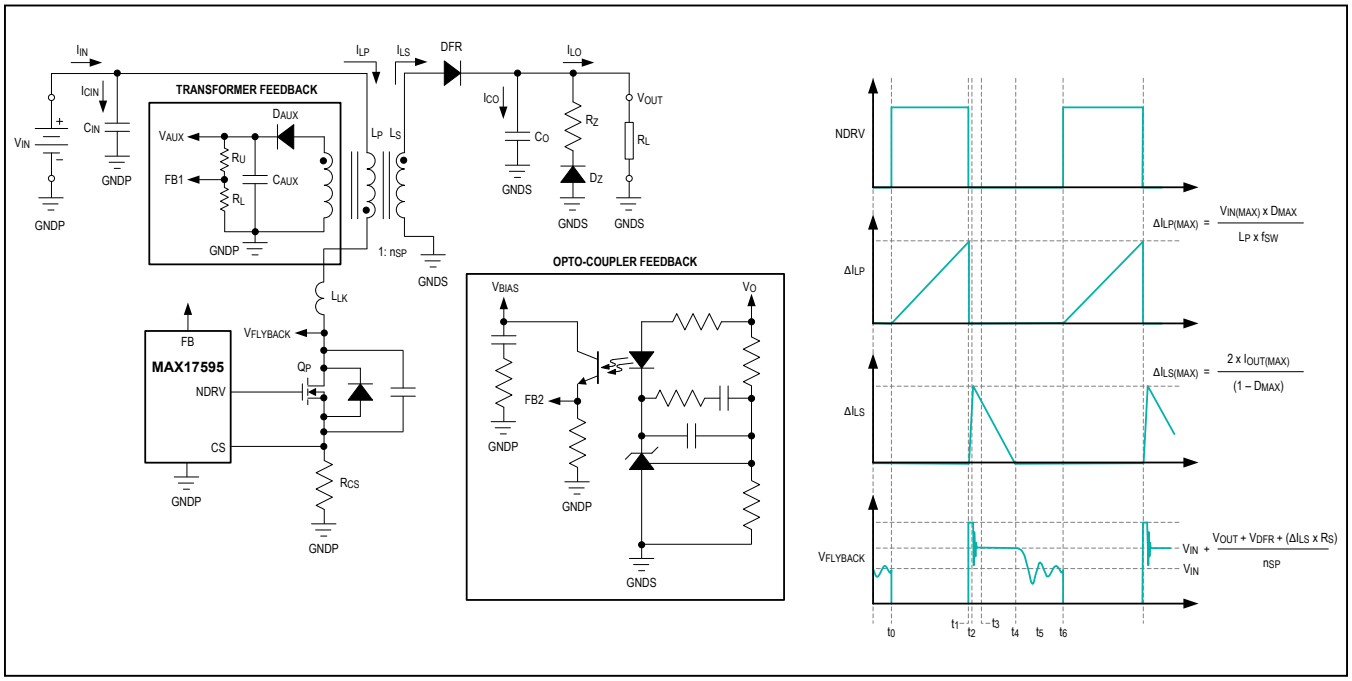

Figure 2. Isolated flyback converter topology with typical waveforms.

By including additional innovative features internally in the MAX17690 no-opto flyback controller, Maxim has enabled power-supply designers to eliminate the additional components, board area, complexity, and cost associated with both the optocoupler and transformer feedback methods. Figure 3 illustrates a simplified schematic and typical waveforms for an isolated no-opto flyback DC-DC converter using the MAX17690.

By comparing Figure 3 with Figure 2, it is evident that there is no difference in the voltage and current waveforms in the traditional and no-opto flyback topologies. The difference is in the control method used to maintain V_{OUT} at its target value over the required load, line, and temperature range. The MAX17690 achieves this with minimum components by forcing the voltage $V_{FLYBACK}$ during the conduction period of the forward rectifying diode (DFR) to be precisely the voltage required to maintain a constant V_{OUT}. When Q_P turns off, the DFR conducts and the drain voltage of Q_P rises to a voltage $V_{FLYBACK}$ above V_{IN}. After initial ringing due to transformer leakage inductance and the junction capacitance of DFR and output capacitance of Q_P, the voltage $V_{FLYBACK}$ is given by:

$$V_{FLYBACK} = V_{IN} + \frac{(V_{OUT} + V_{DFR}(T) + I_{LS}(t) \times R_S(T))}{n_{SP}}$$

where:

$V_{FLYBACK}$ is the Q_P drain voltage relative to primary ground.

$V_{DFR}(T)$ is the forward voltage drop of the DFR, which has a negative temperature coefficient.

$I_{LS}(t)$ is the instantaneous secondary transformer current.

$R_S(T)$ is the total DC resistance of the secondary circuit, which has a positive temperature coefficient.

n_{SP} is the secondary to primary turns ratio of the flyback transformer.

The voltage of interest is ($V_{FLYBACK}$ - V_{IN}), since this is a measure of V_{OUT}. An internal voltage-to-current amplifier generates a current proportional to ($V_{FLYBACK}$ - V_{IN}). This current then flows through R_{SET} to generate a ground referenced voltage (V_{SET}) proportional to ($V_{FLYBACK}$ - V_{IN}). This requires that:

$$\frac{V_{FLYBACK} - V_{IN}}{R_{FB}} = \frac{V_{SET}}{R_{SET}}$$

Combining this equation with the previous equation for $V_{FLYBACK}$, we have:

$$V_{OUT} = V_{SET} \times \left(\frac{R_{FB}}{R_{SET}}\right) \times n_{SP} - V_{DFR}(T) - I_{LS}(t) \times R_S(T)$$

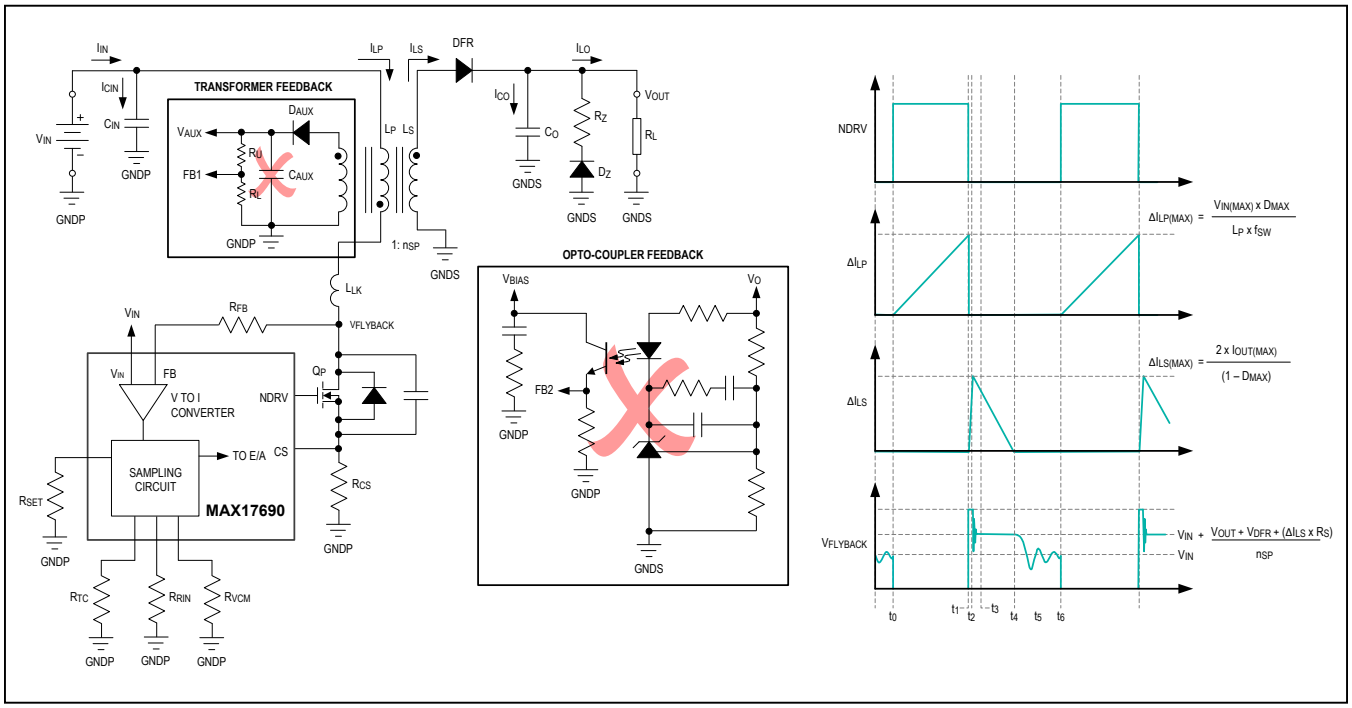

Figure 3. Isolated no-opto flyback converter topology with typical waveforms.

Temperature Compensation

We need to consider the effect of the temperature dependence of V_{DFR} and the time dependence of I_{LS} on the control system. If $V_{FLYBACK}$ is sampled at a time when I_{LS} is very close to zero, then the term $I_{LS}(t) \times R_S(T)$ is negligible and can be assumed to be zero in the previous expression. This is the case when the flyback converter is operating in, or close to, discontinuous conduction mode. It is very important to sample the $V_{FLYBACK}$ voltage before the secondary current reaches zero, since there is a very large oscillation on $V_{FLYBACK}$ due to the resonance between the primary magnetizing inductance of the flyback transformer and the output capacitance of Q_P as soon as the current reaches zero in the secondary, as shown in Figure 2 and Figure 3. The time at which $V_{FLYBACK}$ is sampled is set by resistor R_{VCM}.

The V_{DFR} term has a significant negative temperature coefficient that must be compensated to ensure acceptable output voltage regulation over the required temperature range. This is achieved by internally connecting a positive temperature coefficient current source to the V_{SET} pin. The current is set by resistor R_{TC} connected to ground. The simplest way to understand the temperature compensation mechanism is to think about what needs to happen in the control system when temperature increases. In an uncompensated system, as the temperature increases, V_{DFR} decreases due to its negative temperature coefficient. Since V_{DFR} decreases, V_{OUT} increases by the same amount, therefore $V_{FLYBACK}$ remains unchanged. Since V_{SET} is proportional to $V_{FLYBACK}$, V_{SET} also remains unchanged. Since there is no change in V_{SET}, there is no change in duty cycle demand to bring V_{OUT} back down to its target value. What needs to happen in the temperature compensated case is, when V_{OUT} increases due to the negative temperature coefficient of V_{DFR}, V_{SET} needs to increase by an amount just sufficient to bring V_{OUT} back to its target value. This is achieved by designing V_{SET} with a positive temperature coefficient, expressed mathematically as:

$$\frac{\delta V_{DFR}}{\delta T} \times \frac{1}{n_{SP}} + \frac{\delta V_{TC}}{\delta T} \times \frac{R_{FB}}{R_{TC}} = 0$$

where:

$\delta V_{DFR}/\delta T$ is the diode's forward temperature coefficient

$\delta V_{TC}/\delta T$ = 1.85mV/°C

V_{TC} = 0.55V is the voltage at the TC pin at +25°C

Rearranging the above expression gives:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T}$$

The effect of adding the positive temperature coefficient current (I_{TC}) to the current in R_{FB} is equivalent to adding a positive temperature coefficient voltage in series with V_{DFR} on the secondary side of the value:

$$\frac{V_{TC}}{R_{TC}} \times R_{FB} \times n_{SP}$$

Substituting from the previous expression, this becomes:

$$-V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}}$$

We can now substitute this expression into the expression for V_{OUT} as follows:

$$V_{OUT} = V_{SET} \times \left(\frac{R_{FB}}{R_{SET}}\right) \times n_{SP} - V_{DFR} - V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}}$$

and finally solve for R_{FB}:

$$R_{FB} = \frac{R_{SET}}{n_{SP} \times V_{SET}} \times \left(V_{OUT} + V_{DFR} + V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}}\right)$$

Values for R_{SET}, V_{SET}, and $\delta V_{TC}/\delta T$ can be obtained from the MAX17690 data sheet as follows:

R_{SET} = 10kΩ

V_{SET} = 1V

$\delta V_{TC}/\delta T$ = 1.85mV/°C

Values for V_{DFR} and $\delta V_{DFR}/\delta T$ can be obtained from the output diode data sheet, and n_{SP} is calculated when the flyback transformer is designed.

The value of R_{TC} can then be calculated using the expression from earlier, restated below:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T}$$

The calculated resistor values for R_{FB} and R_{TC} should always be verified experimentally and adjusted, if necessary, to achieve optimum performance over the required temperature range. Note that the reference design described in this document has only been verified at room temperature.

Finally, the internal temperature compensation circuitry requires a current proportional to V_{IN}. R_{RIN} should be chosen as approximately:

$$R_{RIN} = 0.6 \times R_{FB}$$

Setting the $V_{FLYBACK}$ Sampling Instant

The MAX17690 generates an internal voltage proportional to the on-time, volt-second product. This enables the device to determine the correct sampling instant for $V_{FLYBACK}$ during the Q_P off-time. The R_{VCM} resistor is used to scale this internal voltage to an acceptable internal voltage limit in the device.

Design Procedure for No-Opto Flyback Converter Using MAX17690

Now that the principle difference between a traditional isolated flyback converter using optocoupler or auxiliary transformer winding feedback and the isolated no-opto flyback converter using the MAX17690 is understood, a practical design example can be illustrated. The converter design process can be divided into three parts: the power stage design, the setup of the MAX17690 no-opto flyback controller, and closing the control loop. This document is intended to complement the information contained in the MAX17690 data sheet.

The following design parameters are used throughout this document:

SYMBOL	FUNCTION
V_{IN}	Input voltage
V_{UVLO}	Undervoltage turn-on threshold
V_{OVI}	Overvoltage turn-off threshold
t_{SS}	Soft-start time
V_{OUT}	Output voltage
ΔV_O	Steady-state output ripple voltage
I_{OUT}	Output current
P_{OUT}	Output power
$\eta_{(MAX)}$	Target efficiency at maximum load
$\eta_{(MIN)}$	Target efficiency at minimum load
P_{IN}	Input power
f_{SW}	Switching frequency
D	Duty cycle
n_{SP}	Secondary-primary turns ratio

Throughout the design procedure, reference is made to the schematic. See the *Design Resources* section.

Part I: Designing the Power Components

Step 1: Calculate the Minimum Turns Ratio for the Flyback Transformer

The secondary-primary turns ratio (n_{SP}) and the duty cycle (D) for the flyback converter are related by the flyback DC gain function as follows:

$$n_{SP} = \frac{V_{OUT}}{V_{IN}} \times \left(\frac{1-D}{D}\right)$$

The converter's absolute minimum input voltage is the undervoltage lockout threshold (V_{IN} falling), which is programmed with a resistor-divider for the MAX17690. At this voltage and at maximum output power, D should be less than or equal to 66% (the maximum duty cycle at which the MAX17690 can operate) to ensure reliable converter operation. The value of D also determines the ratio of primary and secondary copper and core losses in the flyback transformer. It is advantageous to try make this ratio equal 1 so that the primary and secondary transformer losses are equal. This condition occurs at approximately D = 46%. For the current design, the undervoltage lockout threshold (V_{IN} falling) occurs at 15V, so with D set at 46%, the absolute minimum turns ratio ($n_{SP(MIN)}$) for the flyback transformer is calculated as follows:

$$n_{SP(MIN)} = 0.397$$

For the current design, a transformer turns ratio of $n_{SP} = 0.4$ was chosen.

Step 2: Estimate the Maximum and Minimum Duty Cycle Under Normal Operating Conditions

Normal input voltage operating conditions are defined as $V_{IN(MIN)}$ and $V_{IN(MAX)}$ on page 1. By using the flyback DC gain function again, the duty cycle is estimated as:

$$D = \frac{1}{1 + n_{SP} \times \left(\frac{V_{IN}}{V_{OUT}}\right)}$$

n_{SP} and V_{OUT} are fixed, so clearly D_{MAX} occurs when V_{IN} is a minimum, i.e., at $V_{IN(MIN)}$. For the current design, $V_{IN(MIN)} = 17V$, so:

$$D_{MAX} = 0.42$$

The MAX17690 derives the current, ΔI_{LP}, in the primary magnetizing inductance by measuring the voltage, ΔV_{RCS}, across the current-sense resistor (R_{CS}) during the on-time of the primary-side MOSFET. So:

$$\Delta I_{LP} = \frac{\Delta V_{RCS}}{R_{CS}}$$

ΔI_{LP} is a maximum at D_{MAX} and $V_{IN(MIN)}$ and a minimum at D_{MIN} and $V_{IN(MAX)}$, so:

$$\frac{V_{IN(MIN)}}{L_P} = \frac{\Delta V_{RCS(MIN)} \times f_{SW}}{R_{CS} \times D_{MAX}}$$

and:

$$\frac{V_{IN(MAX)}}{L_P} = \left(\frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{\Delta V_{RCS(MIN)}}{R_{CS}}\right) \times \frac{f_{SW}}{D_{MIN}}$$

Solving these two equations gives:

$$D_{MIN} = D_{MAX} \times \frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \times \frac{\Delta V_{RCS(MIN)}}{\Delta V_{RCS(MAX)}}$$

where $\Delta V_{RCS(MIN)}$ and $\Delta V_{RCS(MAX)}$ correspond to the minimum current limit threshold (20mV) and the maximum current limit threshold (100mV) of the MAX17690, respectively. So, for $V_{IN(MIN)} = 17V$, $V_{IN(MAX)} = 36V$, and $D_{MAX} = 0.42$, we have:

$$D_{MIN} = 0.055$$

Step 3: Calculate the Maximum Allowable Switching Frequency

The isolated no-opto flyback topology requires the primary-side MOSFET to constantly maintain switching, otherwise there is no way to sense the reflected secondary-side voltage at the drain of the primary-side MOSFET. The MAX17690 achieves this by having a critical minimum on-time ($t_{ON(CRIT)}$) for which it drives the MOSFET. At a given switching frequency, $t_{ON(MIN)}$ corresponds to D_{MIN}. From the MAX17690 data sheet, the $t_{ON(CRIT)}$ for the NDRV pin is 235ns. We can, therefore, calculate the maximum allowable switching frequency to ensure that $t_{ON(MIN)} > t_{ON(CRIT)}$ as follows:

$$f_{SW(MAX)} = \frac{D_{MIN}}{t_{ON(CRIT)}} \approx 233.9kHz$$

Since D_{MIN} is fixed by $\Delta V_{RCS(MIN)}$, $\Delta V_{RCS(MAX)}$, D_{MAX}, $V_{IN(MIN)}$, and $V_{IN(MAX)}$, then $t_{ON(MIN)}$ can be chosen arbitrarily larger than $t_{ON(CRIT)}$ so that f_{SW} is less than $f_{SW(MAX)}$. With $t_{ON(MIN)}$ = 403ns, the switching frequency is as follows:

$$f_{SW} = \frac{D_{MIN}}{t_{ON(MIN)}} \approx 128.4kHz$$

Note that the MAX17690 should always be operated in the 50kHz to 250kHz switching frequency range, and $t_{ON(MIN)}$ must be chosen accordingly to ensure that this constraint is met.

Step 4: Estimate the Primary Magnetizing Inductance

Maximum input power is given by:

$$P_{IN(MAX)} = \frac{P_{OUT(MAX)}}{\eta_{MAX}} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX}}$$

For the discontinuous flyback converter, all of the energy stored in the primary magnetizing inductance (L_P) during the MOSFET on-time is transferred to the output during the MOSFET off-time, i.e., the full power transfer occurs during one switching cycle. Therefore, because E = P x t, we have:

$$E_{IN(MAX)} = P_{IN(MAX)} \times \tau_{SW} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

The maximum input energy must be stored in L_P during the on-time of the MOSFET, so:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}^2$$

We also know that the peak current in L_P, $\Delta I_{LP(MAX)}$ occurs at $V_{IN(MIN)}$ and MOSFET on-time $t_{ON(MAX)}$, so:

$$\Delta I_{LP(MAX)}^2 = \frac{V_{IN(MIN)}^2 \times t_{ON(MAX)}^2}{L_P^2}$$

and substituting:

$$E_{IN(MAX)} = \frac{V_{IN(MIN)}^2 \times t_{ON(MAX)}^2}{2 \times L_P}$$

Combining with the original P x t equation gives:

$$\frac{V_{IN(MIN)}^2 \times t_{ON(MAX)}^2}{L_P^2} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

Finally, by rearranging we have an expression for L_P:

$$L_P = \frac{\eta_{MAX} \times V_{IN(MIN)}^2 \times D_{MAX}^2}{2 \times V_{OUT} \times I_{OUT} \times f_{SW}}$$

Estimating the power converter efficiency at 90% and with $V_{IN(MIN)}$ = 17V, D_{MAX} = 0.42, V_{OUT} = 5V, and f_{SW} = 128.4kHz, then:

$$L_{P(MAX)} \approx 19.9\mu H$$

This inductance represents the primary magnetizing inductance at which the calculated D_{MAX} occurs. Choosing a larger inductance will force the converter to operate at a higher D_{MAX} and may cause it to go into continuous conduction mode. Assuming a ±10% tolerance for the primary magnetizing inductance gives:

$$L_P \approx 18\mu H \pm 10\%$$

Step 5: Recalculate D_{MAX}, D_{MIN}, and $t_{ON(MIN)}$ Based on the Selected Value for L_P

Rearranging the L_P equation in Step 4 gives an expression for D_{MAX} as follows:

$$D_{MAX} = \sqrt{\frac{2 \times L_P \times V_{OUT} \times I_{OUT} \times f_{SW}}{\eta_{MAX} \times V_{IN(MIN)}^2}} = 0.4$$

Referring to Step 2:

$$D_{MIN} = D_{MAX} \times \frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \times \frac{\Delta V_{RCS(MIN)}}{\Delta V_{RCS(MAX)}} = 0.052$$

and:

$$t_{ON(MIN)} = \frac{D_{MIN}}{f_{SW}} = 404ns$$

Step 6: Calculate the Peak and RMS Currents in the Primary Winding of the Flyback Transformer

The peak primary winding current occurs at $V_{IN(MIN)}$ and D_{MAX} according to the following equation:

$$\Delta I_{LP(MAX)} = \frac{V_{IN(MIN)} \times D_{MAX}}{L_P \times f_{SW}} \approx 2.69A$$

The RMS primary winding current can be calculated from $\Delta I_{LP(MAX)}$ and D_{MAX} as follows:

$$I_{LP(RMS)} = \Delta I_{LP(MAX)} \times \sqrt{\frac{D_{MAX}}{3}} \approx 0.94A$$

Step 7: Calculate the Peak and RMS Currents in the Secondary Winding of the Flyback Transformer

The peak current in the flyback transformer's secondary-side winding can be established by considering that the entire energy transferred from the primary-side winding to the secondary-side winding is delivered to the load during one switching period. Again, since E = P x t:

$$E_{OUT} = \frac{1}{2} \times L_S \times \Delta I_{LS(MAX)}^2 = P_{OUT} \times \tau_{SW}$$

Substituting:

$$P_{OUT} \times \tau_{SW} = \frac{V_{OUT} \times I_{OUT}}{f_{SW}}$$

And rearranging:

$$\Delta I_{LS(MAX)} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{f_{SW} \times L_P \times n_{SP}^2}} = 6.37A$$

Current flows in the secondary-side winding of the flyback transformer during the time the secondary-side rectifying device is conducting. This conduction time ($t_{ON(SEC)}$) is calculated using the inductor volt-second equation:

$$V = L \times \frac{dI}{dt}$$

where V = V_{OUT}, L = L_S, dI = $\Delta I_{LS(MAX)}$, and dt = $t_{ON(SEC)}$, so:

$$t_{ON(SEC)} = L_S \times \frac{\Delta I_{LS(MAX)}}{V_{OUT}} = L_P \times n_{SP}^2 \times \frac{\Delta I_{LS(MAX)}}{V_{OUT}}$$

The maximum duty cycle of the secondary-side rectifying device ($D_{S(MAX)}$) can now be calculated:

$$D_{S(MAX)} = \frac{t_{ON(SEC)}}{\tau_{SW}} = t_{ON(SEC)} \times f_{SW} = 0.47$$

Finally, the RMS secondary winding current can be calculated from $\Delta I_{LS(MAX)}$ and $D_{S(MAX)}$ as follows:

$$I_{LS(RMS)} = \Delta I_{LS(MAX)} \times \sqrt{\frac{1 - D_{S(MAX)}}{3}} = 2.68A$$

Step 8: Summarize the Flyback Transformer Specification

All the critical parameters for the flyback transformer have been calculated and are summarized below. Using these parameters, a suitable transformer can be designed.

PARAMETER	SYMBOL	VALUE
Primary Magnetizing Inductance	L_P	18µH ±10%
Primary Peak Current	$\Delta I_{LP(MAX)}$	2.69A
Primary RMS Current	$I_{LP(RMS)}$	0.94A
Turns Ratio (N_S/N_P)	n_{SP}	0.4
Secondary Peak Current	$\Delta I_{LS(MAX)}$	6.37A
Secondary RMS Current	$I_{LS(RMS)}$	2.68A

Step 9: Calculate Design Parameters for Secondary-Side Rectifying Device

Depending on the output voltage and current, a choice can be made for the secondary-side rectifying device. Generally, Schottky diodes are used for output voltages above 12V at low currents (less than 1A), and synchronous rectification (MOSFET) is used for voltages less than 12V. The current design is a 5V/1.5A output converter, so we outline a procedure for selecting a suitable MOSFET for the synchronous switch.

Figure 4 shows a simplified schematic with the synchronous MOSFET (Q_S). The MAX17606 is a secondary-side synchronous driver and controller specifically designed for the isolated flyback topology operating in discontinuous conduction mode (DCM) or border conduction mode (BCM).

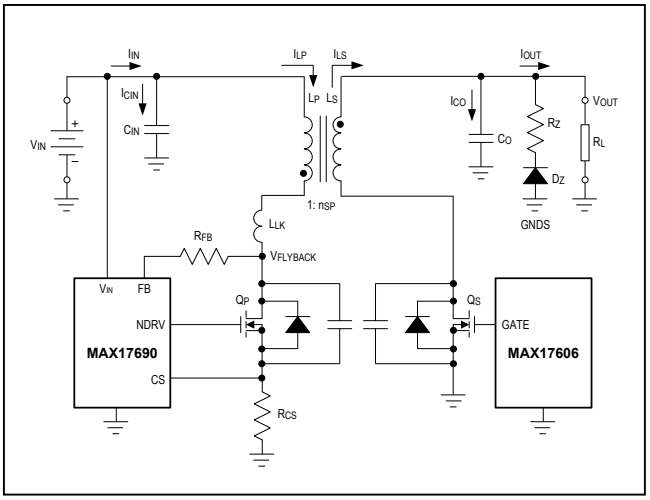

Figure 4. Simplified no-opto flyback schematic with synchronous rectification.

The important parameters to consider for the synchronous rectifying device are the same as those of a regular rectifying diode: peak instantaneous current, RMS current, voltage stress, and power losses. Since Q_S and L_S are in series, they experience the same peak and RMS currents, so:

$$I_{QS(RMS)} = I_{LS(RMS)} = 2.68A$$

and:

$$I_{QS(MAX)} = \Delta I_{LS(MAX)} = 6.37A$$

When Q_S is off, V_{IN} is reflected to the secondary side of the flyback transformer plus (V_{OUT} +$V_{QS(SAT)}$) is applied across the drain-source of Q_S, so:

$$\begin{aligned} V_{QS(MAX)} &= n_{SP} \times V_{IN(MAX)} + V_{OUT} + V_{QS(SAT)} \\ &= 0.4 \times 36V + 5V + (2.68A \times 6.1m\Omega) \\ &\approx 19.4V \end{aligned}$$

Q_S has both conduction losses due to its $R_{DS(ON)}$ and switching losses. Allowing for reasonable design margin, we chose the Infineon® BSZ040N04LS G for this design:

The power losses in the Q_S can be approximated as follows:

$$P_{TOT} = P_{CON} + P_{CDS} + P_{SW} \approx 79mW$$

where:

P_{CON} is the loss due to $I_{QS(RMS)}$ flowing through the drain-source on resistance of Q_S:

$$P_{CON} = I_{QS(RMS)}^2 \times R_{DS(ON)} \approx 44mW$$

P_{CDS} is the loss due to the energy in the drain-source output capacitance being dissipated in Q_S at turn-on:

$$P_{CDS} = \frac{1}{2} \times f_{SW} \times C_{OSS} \times V_{QS(MAX)}^2 \approx 27mW$$

and P_{SW} is the turn-on voltage-current transition loss that occurs as the drain-source voltage decreases and the drain current increases during the turn-on transition:

$$P_{SW} = \frac{1}{2} \times f_{SW} \times I_{QS(t-ON)} \times \left\{ \frac{V_{GS(PL)} - V_{GS(TH)}}{V_{GS(PL)}} \times \left(\frac{Q_{G(T)} + Q_{GD}}{I_{DRV}} \right) \right\} \approx 8mW$$

where I_{DRV} is the maximum drive current capability of the MAX17606's GATE output and $I_{QS(t\text{-}ON)}$ is the instantaneous current in Q_S at turn-on. $I_{QS(t\text{-}ON)}$ is equal to $I_{QS(MAX)}$.

Step 10: Calculate Design Parameters for Primary-Side MOSFET

The important parameters to consider for the primary-side MOSFET (Q_P) are peak instantaneous current, RMS current, voltage stress, and power losses. Because Q_P and L_P are in series, they experience the same peak and RMS currents, so from Step 6:

$$I_{QP(MAX)} = \Delta I_{LP(MAX)} \approx 2.69A$$

and:

$$I_{QP(RMS)} = I_{LP(RMS)} \approx 0.94A$$

When Q_P turns off, V_{OUT} is reflected to the primary side of the flyback transformer, plus $V_{IN(MAX)}$ is applied across the drain source of Q_P. In addition, until Q_S starts to conduct, there is no path for the leakage inductance energy to flow through. This causes the drain-source voltage of Q_P to rise even further. The factor of (1.5) in the equation below represents this additional voltage rise; however, this factor can be higher or lower depending on the transformer and PCB leakage inductances:

$$V_{QP(MAX)} \approx 1.5 \times \left(\frac{V_{OUT} + V_{QS(SAT)}}{n_{SP}} \right) + V_{IN(MAX)} \approx 56V$$

Allowing for reasonable design margin, the Fairchild FDMS86252 was chosen for this design.

The power losses in the Q_P can be approximated as follows:

$$P_{TOT} = P_{CON} + P_{CDS} + P_{SW} \approx 109mW$$

where:

P_{CON} is the loss due to $I_{QP(RMS)}$ flowing through the drain-source on resistance of Q_P:

$$P_{CON} = I_{QP(RMS)}^2 \times R_{DS(ON)} \approx 86mW$$

P_{CDS} is the loss due to the energy in the drain-source output capacitance being dissipated in Q_P at turn-on:

$$P_{CDS} = \frac{1}{2} \times f_{SW} \times C_{OSS} \times V_{QP(MAX)}^2 \approx 23mW$$

And P_{SW} is the turn-on voltage-current transition loss that occurs as the drain-source voltage decreases and the drain current increases during the turn-on transition:

$$P_{SW} = \frac{1}{2} \times f_{SW} \times I_{QP(t-ON)} \times \left\{ \frac{V_{GS(PL)} - V_{GS(TH)}}{V_{GS(PL)}} \times \left(\frac{Q_{G(T)} + Q_{GD}}{I_{DRV}} \right) \right\} \approx 0mW$$

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where I_{DRV} is the maximum drive current capability of the MAX17690's NDRV output and $I_{QP(t-ON)}$ is the instantaneous current in Q_P at turn-on. Because the flyback converter is operating in DCM, $I_{QP(t-ON)}$ is zero and so is P_{SW}.

Step 11: Select the RCD Snubber Components

Referring to Figure 5, when Q_P turns off, I_{LP} charges the output capacitance (C_{OSS}) of Q_P. When the voltage across C_{OSS} exceeds the input voltage plus the reflected secondary to primary voltage, the secondary-side diode (or synchronous switch) turns on. Since the diode (or synchronous switch) is now on, the energy stored in the primary magnetizing inductance is transferred to the secondary; however, the energy stored in the leakage inductance will continue to charge C_{OSS} since there is nowhere else for it to go. Because the voltage across C_{OSS} is the same as the voltage across Q_P, if the energy stored in the leakage inductance charges C_{OSS} to a voltage level greater than the maximum allowable drain-source voltage of Q_P, the MOSFET fails.

One way to avoid this situation arising is to add a suitable resistor-capacitor-diod (RCD) snubber across the transformer's primary winding. In Figure 5, the snubber is labeled R_{SN}, C_{SN}, and D_{SN}. In this situation, when Q_P turns off, the voltage at Node A is:

$$V_{NODEA} = V_{CSN} + V_{IN}$$

When the secondary-side diode (or synchronous switch) turns on, the voltage at Node B is:

$$V_{NODEB} = V_{IN} + \frac{V_{OUT} + V_{DFR}}{n_{SP}}$$

So, the voltage across the leakage inductance is:

$$V_{LLK} = V_{CSN} + V_{IN} - \left(V_{IN} + \frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)$$

$$= V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right) = L_{LK} \times \frac{\Delta I_{SN}}{\Delta t_{SN}}$$

So:

$$\Delta t_{SN} = \frac{L_{LK} \times \Delta I_{SN}}{V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)}$$

The average power dissipated in the snubber network is:

$$P_{SN} = V_{CSN} \times \frac{\Delta I_{SN} \times \Delta t_{SN}}{2 \times \tau_{SW}}$$

Substituting Δt_{SN} into this expression, we have:

$$P_{SN} = \frac{1}{2} \times L_{LK} \times \Delta I_{SN}^2 \times \frac{V_{CSN}}{V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)} \times f_{SW}$$

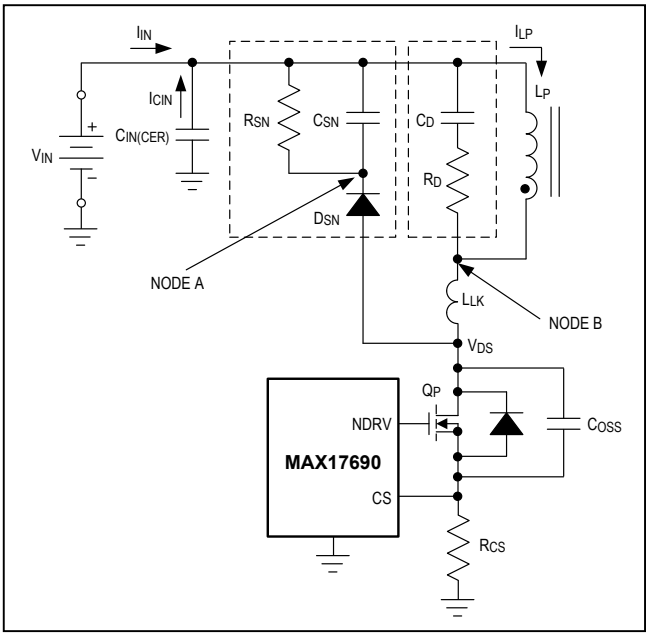

Figure 5. RCD snubber circuit.

The leakage inductance energy is dissipated in R_{SN}, so from:

$$P_{SN} = \frac{V_{CSN}^2}{R_{SN}}$$

We can calculate the required R_{SN} as follows:

$$R_{SN} = \frac{V_{CSN}^2}{\frac{1}{2} \times L_{LK} \times \Delta I_{SN}^2 \times \frac{V_{CSN}}{V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)} \times f_{SW}}$$

Over one switching cycle, we must have:

$$I_{SN} = \frac{V_{CSN}}{R_{SN}} = C_{SN} \times \frac{\Delta V_{SN}}{\tau_{SW}}$$

So, we can calculate the required C_{SN} as follows:

$$C_{SN} = \frac{V_{CSN}}{\Delta V_{CSN} \times R_{SN} \times f_{SW}}$$

Generally, ΔV_{CSN} should be kept to approximately 10% to 30% of V_{CSN}. Figure 6 illustrates V_{CSN}, ΔI_{SN}, and Δt_{SN}. The voltage across the snubber capacitor (V_{CSN}) should be selected so that:

$$V_{CSN} < V_{DSMAX(QP)} - V_{IN(MAX)}$$

Choosing too large a value for V_{CSN} causes the voltage on the Q_P drain to get too close to its maximum allowable drain-source voltage, while choosing too small a value results in higher power losses in the snubber resistor. A reasonable value should result in a maximum drain voltage on Q_P that is approximately 75% of its maximum

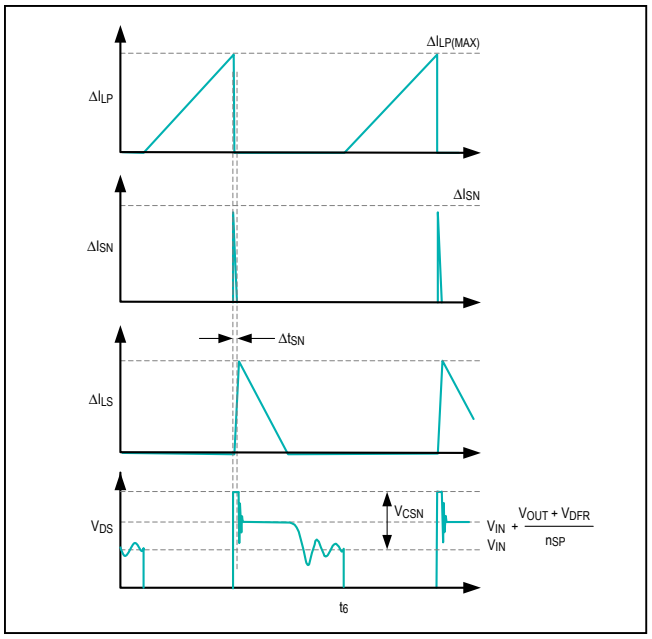

Figure 6. RCD snubber circuit waveforms.

allowable value. The worst-case condition for the snubber circuit occurs at maximum output power when:

$$\Delta I_{SN} = \Delta I_{LP(MAX)}$$

Assuming the leakage inductance is 3.0% of the primary inductance, choosing V_{CSN} = 23V and ΔV_{CSN} = 3.9V, we get the following approximate values:

$$P_{SN} = 553mW$$

$$R_{SN} = 1k\Omega$$

$$C_{SN} = 47nF$$

Finally, we consider the snubber diode (D_{SN}). This diode should have at least the same voltage rating as the MOSFET, Q_P. Although the average forward current is very low, it must have a peak repetitive current rating greater than $\Delta I_{LP(MAX)}$.

Step 12: Calculate the Required Current-Sense Resistor

From Step 4, we have the maximum input power given by:

$$P_{IN(MAX)} = \frac{P_{OUT(MAX)}}{\eta_{MAX}} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX}}$$

For the DCM flyback converter, all the energy stored in the primary magnetizing inductance (L_P) during the MOSFET on-time is transferred to the output during the MOSFET off-time, i.e., the full power transfer occurs during one switching cycle. Therefore, since E = P x t, we have:

$$E_{IN(MAX)} = P_{IN(MAX)} \times \tau_{SW} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

The maximum input energy must be stored in L_P during the primary-side MOSFET on-time, so:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}^2$$

Substituting the equations above:

$$\frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}^2 = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

and:

$$\Delta I_{LP} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta_{MAX} \times L_P \times f_{SW}}}$$

From Step 2, we have:

$$\Delta I_{LP} = \frac{\Delta V_{RCS}}{R_{CS}}$$

so:

$$R_{CS} = \Delta V_{RCS} \times \sqrt{\frac{\eta_{MAX} \times L_P \times f_{SW}}{2 \times V_{OUT} \times I_{OUT}}} = 37m\Omega$$

A standard 36mΩ resistor was chosen for R_{CS}.

Step 13: Calculate and Select the Input Capacitors

Figure 7 shows a simplified schematic of the primary side of the flyback converter and the associated current waveforms. In steady-state operation, the converter draws a pulsed high-frequency current from the input capacitor (C_{IN}). This current leads to a high-frequency ripple voltage across the capacitor according to the following expression:

$$I_{CIN} = C_{IN} \times \frac{\Delta V_{CIN}}{\Delta t}$$

It is the ripple voltage arising from the amp-second product through C_{IN}.

During the Q_P on-time interval from t_0 to t_1, the capacitor is supplying current to the primary inductance (L_P) of the flyback transformer and its voltage is decreasing. During the Q_P off-time time interval from t_1 to t_2, no current is flowing in L_P, and current is being supplied to capacitor from V_{IN}. According to the charge balance law, the decrease in capacitor voltage during time t_0 to t_1 must equal the increase in capacitor voltage during time t_1 to t_2. So:

$$I_{CIN[t_1-t_2]} = C_{IN} \times \frac{\Delta V_{CIN}}{(t_2 - t_1)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

And finally, since:

$$\frac{1}{(t_2 - t_1)} = \frac{f_{SW}}{(1 - D_{MAX})}$$

we have:

$$C_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}} \times \frac{1}{\Delta V_{CIN}} \times \frac{(1 - D_{MAX})}{f_{SW}}$$

For maximum high-frequency ripple voltage requirement ΔV_{CIN}, we can now calculate the required minimum C_{IN}.

There is high-frequency AC current flowing in C_{IN}, as shown in the center waveform of Figure 7. The selected capacitor must be specified to tolerate the maximum RMS current ($I_{CIN(RMS)}$). From the simplified schematic:

$$I_{LP} = I_{IN} + I_{CIN}$$

Therefore:

$$I_{CIN(RMS)} = \sqrt{I_{LP(RMS)}^2 - I_{IN(RMS)}^2}$$

where:

$$I_{IN(RMS)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

and from Step 6:

$$I_{LP(RMS)} = \Delta I_{LP(MAX)} \times \sqrt{\frac{D_{MAX}}{3}}$$

So:

$$I_{CIN(RMS)} = \sqrt{\frac{D_{MAX}}{3} \times \Delta I_{LP(MAX)}^2 - \frac{V_{OUT}^2 \times I_{OUT}^2}{\eta_{MAX}^2 \times V_{IN(MIN)}^2}} \approx 0.85 A_{RMS}$$

An additional high-frequency ripple voltage is present due to this RMS current flowing through the ESR of the capacitor. Ceramic capacitors are generally used for limiting high-frequency ripple due to their high AC current capability and low ESR.

In addition to using a ceramic capacitor for high-frequency input ripple-voltage control as described above, an electrolytic capacitor is sometimes inserted at the input of a flyback converter to limit the input voltage deviation when there is a rapid output load change. A 100% load change gives rise to an input current transient of:

$$\Delta I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

During this transient, there is a voltage drop across any series stray inductance ($L_{IN(STRAY)}$), that exists between V_{IN} and C_{IN} of the power supply. So from:

$$\frac{1}{2} \times C_{IN} \times \Delta V_{CIN}^2 = \frac{1}{2} \times L_{IN(STRAY)} \times \Delta I_{IN}^2$$

we have:

$$C_{IN} = L_{IN(STRAY)} \times \frac{\Delta I_{IN(MAX)}^2}{\Delta V_{CIN}^2}$$

We now have two values for C_{IN}. One for input high-frequency ripple-voltage control:

$$C_{IN(CER)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}} \times \frac{1}{\Delta V_{CIN}} \times \frac{(1 - D_{MAX})}{f_{SW}}$$

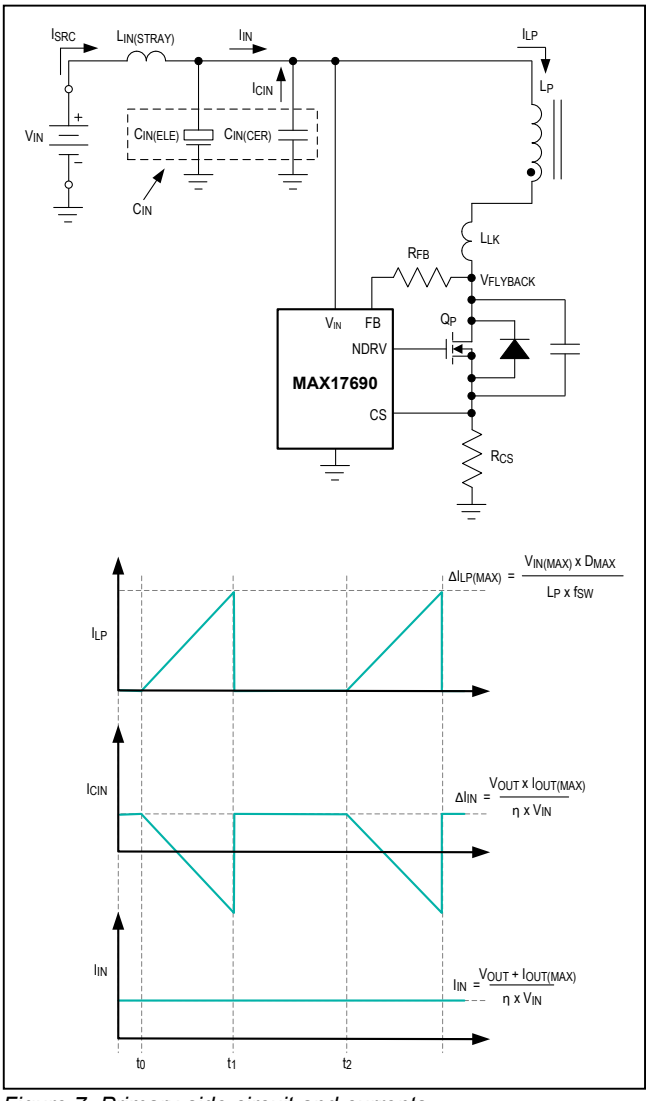

Figure 7. Primary-side circuit and currents.

and a second for transient input voltage control:

$$C_{IN(ELE)} = L_{IN(STRAY)} \times \frac{\Delta I_{IN(MAX)}^{2}}{\Delta V_{CIN}^{2}}$$

If $C_{IN(ELE)} > C_{IN(CER)}$, both ceramic and electrolytic capacitors must be used at the input of the power supply and ΔV_{CIN} should be limited to approximately 75mV to keep the AC current in the ESR of the electrolytic capacitor within acceptable limits. Otherwise, $C_{IN(ELE)}$ is not required. In this case, the value of $C_{IN(CER)}$ can be significantly reduced since there is no longer any requirement to limit ΔV_{CIN} to less than 75mV. Based on the current design specification with $L_{IN(STRAY)}$ approximated at 50nH, we have:

$$C_{IN(CER)} = 32.3\mu F$$

and:

$$C_{IN(ELE)} = 2.5\mu F$$

Since $C_{IN(ELE)} < C_{IN(CER)}$, an electrolytic capacitor is not required. We can now recalculate $C_{IN(CER)}$ based on a ΔV_{CIN} = 420mV:

$$C_{IN(CER)} \approx 5.8\mu F$$

Allowing for a ±10% capacitor tolerance and a further reduction of capacitance of 48% due to the DC bias effect (operating a 50V ceramic capacitor at 36V), our final nominal value of input capacitance required is:

$$C_{IN(CER)} = \frac{5.8\mu F}{90\% \times 52\%} \approx 12.4\mu F$$

This is achieved by using two 10µF ceramic capacitors (Murata GRM32ER71H106KA12) in parallel. The AC current in each capacitor is:

$$\frac{I_{CIN(RMS)}}{2} \approx 0.43A_{RMS}$$

which is well within specification for the selected capacitor.

Step 14: Calculate and Select the Output Capacitor

High-frequency ripple voltage requirements are also used to determine the value of the output capacitor (C_O) in a flyback converter. Figure 8 shows a simplified schematic of the secondary side of the flyback converter and the associated current waveforms.

In steady-state operation, the load draws a DC current from the secondary side of the flyback converter. By examining the secondary current waveforms, we see that C_O is supplying the full output current I_{OUT} to the load during the time interval from t_2 to t_3. During this time interval, the voltage across C_O decreases. At time t_3, Q_P has just turned off and the secondary rectifying diode DFR (or the secondary synchronous switch Q_S) starts to conduct

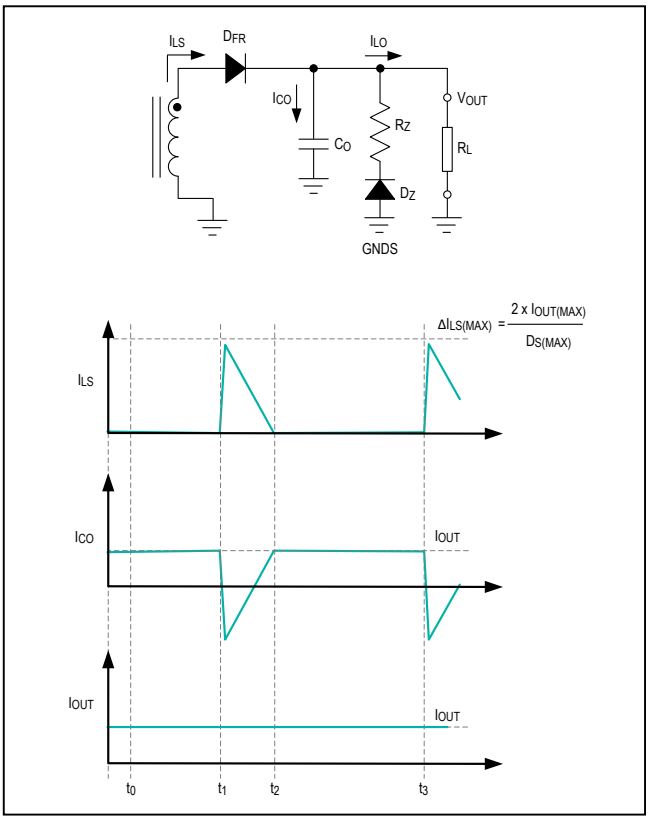

Figure 8. Secondary-side circuit and currents.

supplying current to the load and to C_O. The charging and discharging of C_O leads to a high-frequency ripple voltage at the output according to the following expression:

$$I_{CO} = C_O \times \frac{\Delta V_{CO}}{\Delta t}$$

Again, as with C_{IN}, this is the ripple voltage arising from the amp-second product through C_O.

By the capacitor charge balance law, the decrease in capacitor voltage during time t_2 to t_3 must equal the increase in capacitor voltage during time t_1 to t_2. When the capacitor is discharging, we have:

$$I_{CO[t_2-t_3]} = C_O \times \frac{\Delta V_{CO}}{(t_3 - t_2)} = I_{OUT}$$

Finally, since:

$$\frac{1}{(t_3 - t_2)} = \frac{f_{SW}}{(1 - D_{S(MAX)})}$$

we have:

$$C_O = I_{OUT} \times \frac{1}{\Delta V_{CO}} \times \frac{(1 - D_{S(MAX)})}{f_{SW}}$$

For maximum high-frequency ripple voltage requirement ΔV_{CO}, we can now calculate the required minimum C_O:

$$C_O \approx 120.6\mu F$$

As with C_{IN}, an additional high-frequency ripple voltage occurs at the output due to the ESR of C_O and can be minimized by choosing a capacitor with low ESR.

Also, as with C_{IN}, there is high-frequency AC current flowing in C_O, as shown in the center waveform of Figure 8. The selected capacitor must be specified to tolerate this maximum RMS current ($I_{CO(RMS)}$). From the simplified schematic:

$$I_{LS} = I_{OUT} + I_{CO}$$

Therefore:

$$I_{CO(RMS)} = \sqrt{I_{LS(RMS)}^2 - I_{OUT(RMS)}^2}$$

where:

$$I_{OUT(RMS)} = I_{OUT}$$

and from Step 7:

$$I_{LS(RMS)} = \Delta I_{LS(MAX)} \times \sqrt{\frac{1 - D_{S(MAX)}}{3}}$$

so:

$$I_{CO(RMS)} = \sqrt{\frac{1 - D_{S(MAX)}}{3} \times \Delta I_{LS(MAX)}^2 - I_{OUT}^2} \approx 2.22A_{RMS}$$

If we allow for a ±20% capacitor tolerance and a further reduction of capacitance of 57% due to the DC bias effect (operating a 6.3V ceramic capacitor at 5V), our final nominal value is:

$$C_O = \frac{120.6\mu F}{80\% \times 43\%} \approx 350\mu F$$

We can achieve this by placing four 100µF ceramic capacitors (Murata GRM32ER60J107ME20) in parallel. The minimum output capacitance using the above combination is 137.6µF. The AC current in each capacitor is:

$$\frac{I_{CO(RMS)}}{4} \approx 0.55A_{RMS}$$

which is well within specification for the selected capacitor.

Step 15: Summarize the Power Component Design

A first pass at calculating the power components in the no-opto flyback converter using the MAX17690 has been completed. Referring to the schematic, a summary of the power components is listed as follows:

POWER COMPONENT	QTY	DESCRIPTION
Flyback Transformer	1	PRI. INDUCTANCE = 18µH SEC-PRI TURNS RATIO = 0.4 PEAK. PRI CURRENT = 2.69A PRI. RMS CURRENT = 0.94A PEAK SEC. CURRENT = 6.37A SEC. RMS CURRENT = 2.68A SWITCHING FREQ. = 128.4kHz
Input Capacitors	2	CAPACITOR; SMT (1210); CERAMIC CHIP 10µF; 50V; 10%; X7R Murata GRM32ER71H106KA12
Output Capacitors	4	CAPACITOR; SMT (1210); CERAMIC CHIP 100µF; 6.3V; 20%; X5R Murata GRM32ER60J107ME20
Primary MOSFET	1	MOSFET; NCH; I-(16A); V-(150V) Fairchild FDMS86252
Synchronous MOSFET	1	MOSFET; NCH; I-(40A); V-(40V) Infineon BSZ040N04LS G

Part II: Setting Up the MAX17690 No-Opto Flyback Controller

Step 16: Setting Up the Switching Frequency

The MAX17690 can operate at switching frequencies between 50kHz and 250kHz (subject to the considerations in Step 3). A lower switching frequency optimizes the design for efficiency, whereas increasing the switching frequency allows for smaller inductive and capacitive components sizes and costs. A switching frequency of 143.5kHz was chosen in Step 3. R9 sets the switching frequency as follows:

$$R9 = \frac{5 \times 10^6}{f_{SW}} \approx 39k\Omega$$

where R9 is in kΩ and f_{SW} is in Hz.

Step 17: Setting Up the Soft-Start Time

The capacitor C6 connected between the SS pin and SGND programs the soft-start time. A precision internal 5µA current source charges the soft-start capacitor C6. During the soft-start time, the voltage at the SS pin is used as a reference for the internal error amplifier during start-up. The soft-start feature reduces inrush current during startup. Since the reference voltage for the internal error amplifier is ramping up linearly, so too is the output voltage during soft-start. The soft-start capacitor is chosen based on the required soft-start time (10ms) as follows:

$$C6 = 5 \times t_{SS} \approx 50nF$$

where C6 is in nF and t_{SS} is in ms. A standard 47nF capacitor was chosen.

Step 18: Setting Up the UVLO and OVI Resistors

A resistor-divider network of R1, R3, and R2 from V_{IN} to SGND sets the input undervoltage lockout threshold and the output overvoltage inhibit threshold. The MAX17690 does not commence its startup operation until the voltage on the EN/UVLO pin (R3/R2 node) exceeds 1.215V (typ). When the voltage on the OVI pin (R1/R3 node) exceeds 1.215V (typ), the MAX17690 stops switching, thus inhibiting the output. Both pins have hysteresis built in to avoid unstable turn-on/turn-off at the UVLO/EN and OVI thresholds. After the device is enabled, if the voltage on the UVLO/EN pin drops below 1.1V (typ), the controller turns off; after the device is OVI inhibited, it turns back on when the voltage at the OVI pin drops below 1.1V (typ). Whenever the controller turns on, it goes through the soft-start sequence. For the current design R1 = 10kΩ, R2 = 280kΩ, and R3 = 12.7kΩ give rise to an UVLO/EN threshold of 16.2V and an OVI threshold of 36.8V.

Step 19: Placing Decoupling Capacitors on V_{IN} and INTVCC Pins

As previously discussed, the MAX17690 no-opto flyback controller compares the voltage $V_{FLYBACK}$ to V_{IN}. This voltage difference is converted to a proportional current that flows in R5. The voltage across R5 is sampled and compared to an internal reference by the error amplifier. The output of the error amplifier is used to regulate the output voltage. The V_{IN} pin should be directly connected to the input voltage supply. For robust and accurate operation, a ceramic capacitor (C2 = 1µF) should be placed between V_{IN} and SGND as close as possible to the IC.

V_{IN} powers the MAX17690's internal low dropout regulator. The LDO's regulated output is connected to the INTVCC pin. A ceramic capacitor (C3 = 2.2µF, min) should be connected between the INTVCC and PGND pins for the stable operation over the full temperature range. Place this capacitor as close as possible to the IC.

Step 20: Setting Up the Feedback Components

R_{SET} (R5), R_{FB} (R4, R18), R_{RIN} (R8), R_{VCM} (R6), and R_{TC} (R7) are critically important to achieving optimum output voltage regulation across all specified line, load, and temperature ranges.

R_{SET} resistor (R5): This resistor value is optimized based on the IC's internal voltage to current amplifier and should not be changed.

$$R5 = R_{SET} = 10k\Omega$$

R_{FB} resistor (R4, R18): The feedback resistor is calculated according to the following equation:

$$R_{FB} = \frac{R_{SET}}{n_{SP} \times V_{SET}} \times \left(V_{OUT} + V_{DFR} + V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}} \right)$$

Since we are using a synchronous MOSFET for rectification on the secondary side, we can assume that $\delta V_{DFR}/\delta T = 0$, so:

$$R_{FB} = \frac{R_{SET}}{n_{SP} \times V_{SET}} \times (V_{OUT} + V_{DFR}) \approx 126k\Omega$$

From the MAX17690 data sheet, V_{SET} = 1V. The two resistors R4 = 121kΩ and R18 = 4.99kΩ form R_{FB}. Using one high-value resistor and one low-value resistor in series allows slight adjustment to the series resistance combination so that the output voltage can be fine-tuned to its required value, if necessary.

R_{RIN} resistor (R8): The internal temperature compensation circuitry requires a current proportional to V_{IN}. R_{RIN} establishes this current and is calculated according to the following equation:

$$R_{RIN} \approx 0.6 \times R_{FB}$$

R_{VCM} resistor (R6): The MAX17690 generates an internal voltage proportional to the on-time, volt-second product. This enables the device to determine the correct sampling instant for $V_{FLYBACK}$ during the Q_P off-time. Resistor R6 is used to scale this internal voltage to an acceptable internal voltage limit in the device. To calculate the resistor, we must first calculate a scaling constant as follows:

$$K_C = \frac{(1 - D_{MAX}) \times 10^8}{3 \times f_{SW}} = 165$$

After K_C is calculated, the R6 value can be selected from the table below by choosing the resistance value that corresponds to the next largest K_C.

K_C	R6
640	0Ω
320	75kΩ
160	121kΩ
80	220Ω
40	Open

In the present case, R6 = 75kΩ.

R_{TC} resistor (R7): The value of R_{TC} can then be calculated using the previous expression, restated below:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T}$$

Since we are using a synchronous MOSFET for secondary-side rectification, we can assume that the temperature coefficient $\delta V_{DFR}/\delta T$ is zero, so R_{TC} should be infinite (i.e., open circuit).

This completes the setup of the MAX17690 no-opto flyback controller.

Part III: Closing the Control Loop

Step 21: Determine the Required Bandwidth

The bandwidth of the control loop determines how quickly the converter can respond to changes at its input and output. If we have a step change in output current, the voltage across C_O decreases, as shown in Figure 9.

The control loop detects this reduction in output voltage and increases the duty cycle of Q_P to supply more current to C_O. The amount of time required by the control loop to increase the duty cycle from its minimum value to its maximum value is the response time (τ_{RES}) of the control loop. For the MAX17690, we have:

$$\tau_{RES} \approx \left\{\frac{1}{3 \times f_C} + \frac{1}{f_{SW}}\right\}$$

where f_C is the bandwidth of the power converter. If we apply a switching load step of amplitude ΔI_{STEP} at a frequency of ($1/\tau_{RES}$) and a 50% duty cycle then, to limit the output voltage deviation to $\pm\Delta V_{OUT(STEP)}$, we must have a minimum output capacitance of:

$$C_{O(MIN)} = \frac{\Delta I_{OUT(STEP)} \times \left(\frac{\tau_{RES}}{2}\right)}{\Delta V_{OUT(STEP)}}$$

Combining the two previous equations, we have:

$$f_C = \frac{\frac{1}{3} \times f_{SW} \times \Delta I_{OUT(STEP)}}{2 \times f_{SW} \times C_{O(MIN)} \times \Delta V_{OUT(STEP)} - \Delta I_{OUT(STEP)}}$$

It is normal to specify $\Delta V_{OUT(STEP)}$ for a load step from 50% to 100% of the maximum output current. We have already calculated $C_{O(MIN)}$ = 137.6µF in Step 14, f_{SW} = 128.4kHz, so based on a 3% maximum $\Delta V_{OUT(STEP)}$:

$$f_C \approx 7.1kHz$$

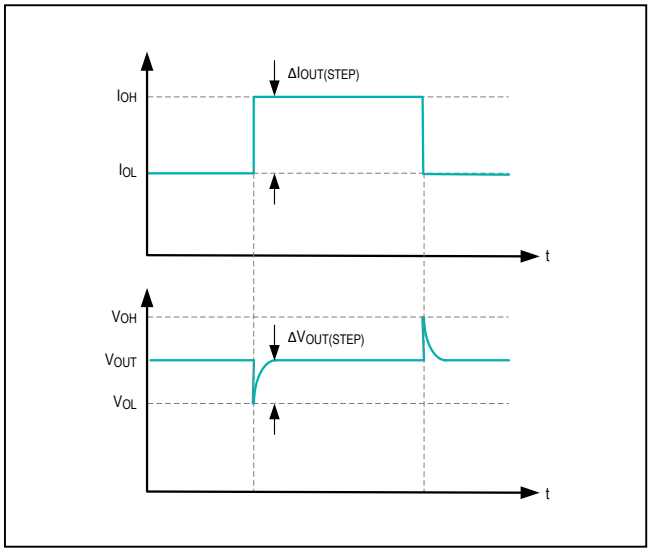

Figure 9. Output load step response.

Step 22: Calculate the Loop Compensation

The MAX17690 uses peak current-mode control and an internal transconductance error amplifier to compensate the control loop. The control loop is modeled, as shown in Figure 10, by a power modulator transfer function ($G_{MOD(S)}$), an output-voltage feedback transfer function ($G_{FB(S)}$), and an error amplifier transfer function ($G_{EA(S)}$).

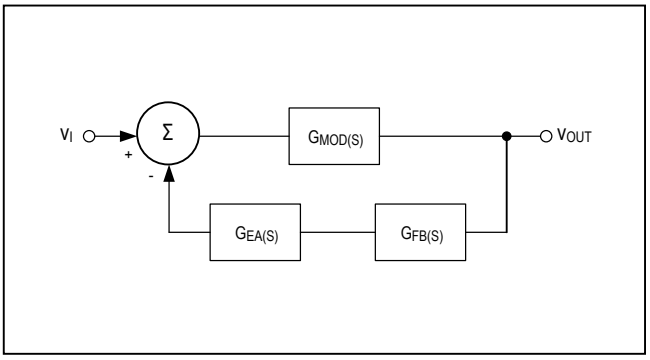

Figure 10. Simplified model of control loop.

The power modulator has a pole located at $f_{P(MOD)}$ determined by the impedance of C_O and the load impedance R_L. It also has a zero at $f_{Z(MOD)}$ determined by the impedance of C_O and the ESR of C_O. The DC gain of the power modulator is determined by the peak primary current ΔI_{LP} and R_{CS}. So:

$$G_{MOD(DC)} = \frac{1}{\Delta I_{LP} \times R_{CS}}$$

$$f_{P(MOD)} = \frac{1}{2\pi \times C_O \times R_L} = \frac{I_{OUT}}{2\pi \times C_O \times V_{OUT}}$$

and:

$$f_{Z(MOD)} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

The output voltage feedback transfer function $G_{FB(S)}$ is independent of frequency and has a DC gain determined by V_{IN}, $V_{FLYBACK}$, and V_{SET} as follows:

$$G_{FB(DC)} = \frac{V_{SET}}{V_{FLYBACK} - V_{IN}} = \frac{V_{SET} \times n_{SP}}{V_{OUT} + V_{DFR}}$$

The MAX17690's transconductance error amplifier should be set up in a configuration to compensate for the pole at $f_{P(MOD)}$ and the zero at $f_{Z(MOD)}$ of the modulator. This can be achieved by a Type II transconductance error amplifier compensation shown in Figure 11.

This compensation scheme type has a low frequency pole at $f_{P-LF(EA)}$ due to the very large output resistance R_O (30MΩ to 50MΩ) of the operational transconductance amplifier (OTA). It has a zero at $f_{Z(EA)}$ determined by C_Z and R_Z of the compensation network, and it has an

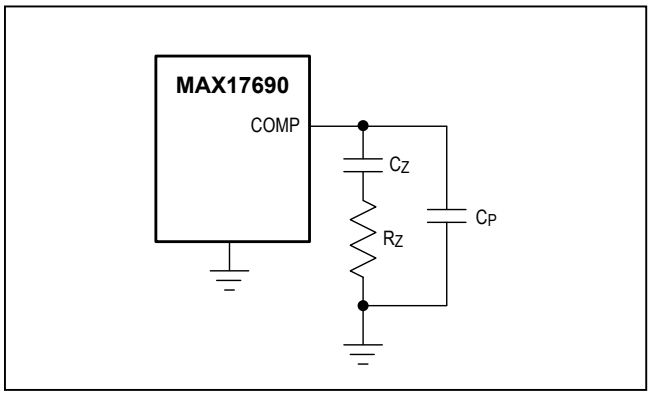

Figure 11. Type II compensation for OTA.

additional pole at $f_{P(EA)}$ determined by C_P and R_Z of the compensation network. So:

$$f_{P-LF(EA)} = \frac{1}{2\pi \times C_Z \times (R_O + R_Z)}$$

$$f_{Z(EA)} = \frac{1}{2\pi \times C_Z \times R_Z}$$

and:

$$f_{P(EA)} = \frac{1}{2\pi \times C_P \times R_Z}$$

To achieve stable operation, we must ensure that:

$$f_{P(MOD)} \ll f_C < \frac{f_{SW}}{20}$$

Set the closed-loop gain at f_C equal to 1:

$$G_{MOD(f_C)} \times G_{FB(f_C)} \times G_{EA(f_C)} = 1$$

Place the zero in the error amplifier network at the same frequency as the pole in the power modulator transfer function:

$$f_{Z(EA)} = f_{P(MOD)}$$

$$\frac{1}{2\pi \times C_Z \times R_Z} = \frac{I_{OUT}}{2\pi \times C_O \times V_{OUT}}$$

The frequency $f_{Z(MOD)}$ at which the zero occurs in the power modulator transfer function depends on the ESR of C_O. If ceramic capacitors are used for C_O, $f_{Z(MOD)}$ will be generally much higher than f_C. However, if the ESR of C_O is large, $f_{Z(MOD)}$ could be lower than f_C. This is a very important point, since both the gain of the power modulator at f_C and the gain of the error amplifier at f_C depend on whether $f_{Z(MOD)}$ is greater than or less than f_C. This is illustrated in Figure 12.

By examining the gain plots in Figure 12, we see that for $f_{Z(MOD)} > f_C$:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \left(\frac{f_{P(MOD)}}{f_C} \right)$$

$$G_{EA(f_C)} = g_{m(EA)} \times R_Z$$

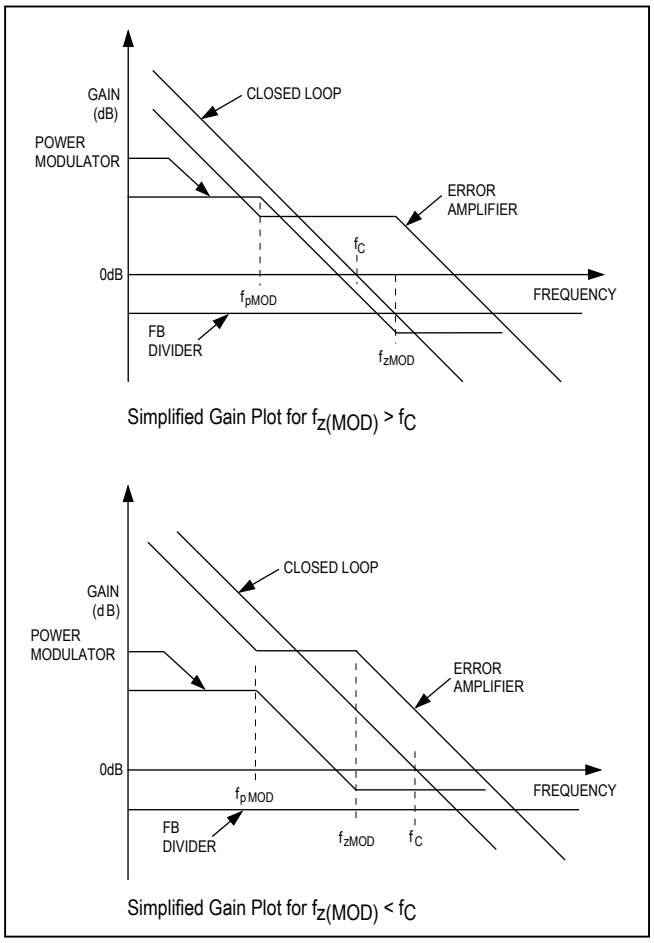

Figure 12. Simplified gain plot.

and for $f_{Z(MOD)} < f_C$:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \left(\frac{f_{P(MOD)}}{f_{Z(MOD)}} \right)$$

$$G_{EA(f_C)} = g_{m(EA)} \times \left(\frac{f_{Z(MOD)}}{f_C} \right) \times R_Z$$

For the current design, we have:

$$f_{P(MOD)} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_O} \approx 347Hz$$

and:

$$f_{Z(MOD)} = \frac{1}{2\pi \times ESR_{CO} \times C_O} \approx 4.6MHz$$

Since $f_{Z(MOD)} > f_C$:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \left(\frac{f_{P(MOD)}}{f_C} \right) = \frac{1}{\Delta I_{LP} \times R_{CS}} \times \left(\frac{f_{P(MOD)}}{f_C} \right)$$

$$G_{EA(f_C)} = g_{m(EA)} \times R_Z$$

and since G_{FB} is independent of frequency, we have:

$$G_{FB(f_C)} = G_{FB(DC)} = \frac{V_{SET} \times n_{SP}}{V_{OUT} + V_{DFR}}$$

We can now set the closed-loop gain equal to 1 as follows:

$$G_{MOD(f_C)} \times G_{FB(DC)} \times G_{EA(f_C)} = 1$$

$$\frac{1}{\Delta I_{LP} \times R_{CS}} \times \left(\frac{f_{P(MOD)}}{f_C} \right) \times \frac{V_{SET} \times n_{SP}}{V_{OUT} + V_{DFR}} \times g_{m(EA)} \times R_Z = 1$$

Rearranging we can calculate:

$$R_Z = \frac{1}{g_{m(EA)}} \times \frac{(V_{OUT} + V_{DFR})}{V_{SET} \times n_{SP}} \times \left(\frac{f_C}{f_{P(MOD)}} \right) \times R_{CS} \times \Delta I_{LP}$$

Substituting ΔI_{LP} from Step 12:

$$R_Z = \frac{1}{g_{m(EA)}} \times \frac{(V_{OUT} + V_{DFR})}{V_{SET} \times n_{SP}} \times \left(\frac{f_C}{f_{P(MOD)}} \right) \times R_{CS} \times \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta_{MAX} \times L_P \times f_{SW}}}$$

$$= 7.7k\Omega$$

Finally, we can calculate the remaining components, C_Z and C_P, in the error amplifier compensation network as follows:

$$C_Z = \frac{1}{2\pi \times f_{P(MOD)} \times R_Z} = 60nF$$

and:

$$C_P = \frac{1}{2\pi \times f_{Z(MOD)} \times R_Z} = 4pF$$

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—