59.4W, No-Opto Flyback DC-DC Converter Using MAX17690

MAXREFDES1040

Introduction

The MAX17690 is a peak current mode, fixed-frequency switching controller specifically designed for the isolated flyback topology operating in Discontinuous Conduction Mode (DCM). The device senses the isolated output voltage directly from the primary-side flyback waveform during the off-time of the primary switch. No auxiliary winding or optocoupler is required for output voltage regulation.

The MAX17690 is designed to operate over a wide supply range from 4.5V to 60V. The switching frequency is programmable from 50kHz to 250kHz. The MAX17690 provides an input overvoltage protection through the OVI pin. The 7V internal LDO output of the MAX17690 makes it suitable for switching both logic-level and standard MOSFETs used in flyback converters. With 2A/4A source/sink currents, the MAX17690 is ideal for driving low $R_{DS(ON)}$ power MOSFETs with fast gate transition times. The MAX17690 provides an adjustable soft-start feature to limit the inrush current during startup.

The MAX17690 provides temperature compensation for the output diode forward-voltage drop. The MAX17690 has robust hiccup-protection and thermal protection schemes, and is available in a space-saving 3mm x 3mm 16-pin TQFN package with a temperature range from -40°C to +125°C.

- No Optocoupler or Third Winding Required
- 2A/4A Peak Source/Sink Gate Drive Currents
- 50kHz to 250kHz Programmable Switching Frequency
- Input EN/UVLO Feature
- Input Overvoltage Protection
- Programmable Soft-Start
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown Protection
- -40°C to +125°C Operating Temperature Range
- Space-Saving, 3mm x 3mm, 16-Pin TQFN Package

Hardware Specification

A no-opto flyback DC-DC converter using the MAX17690 is demonstrated for a 54V DC output application. The power supply delivers up to 1.1A at 54V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	18V	60V
Frequency	f_{SW}	125kHz	
Maximum Efficiency	η	91%	
Output Voltage	V_{OUT}	54V	
Output Current	I_{OUT}	0A	1.1A
Output Power	P_{OUT}	59.4W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a no-opto flyback using Maxim's MAX17690 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

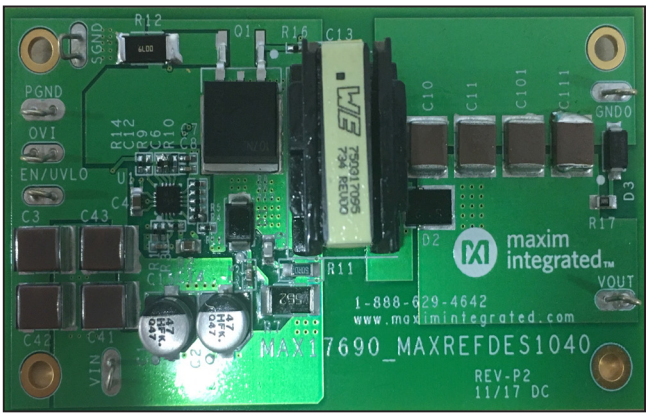

Figure 1. MAXREFDES1040 hardware.

Generic Isolated Power Supply

Figure 2 shows a generic isolated power-supply block diagram. It consists of a power stage, an isolation transformer, rectifier, secondary-side error amplifier, and opto-coupler to provide a feedback for the primary side control. Different isolated power supplies are different depending upon how the transformer is being used in them.

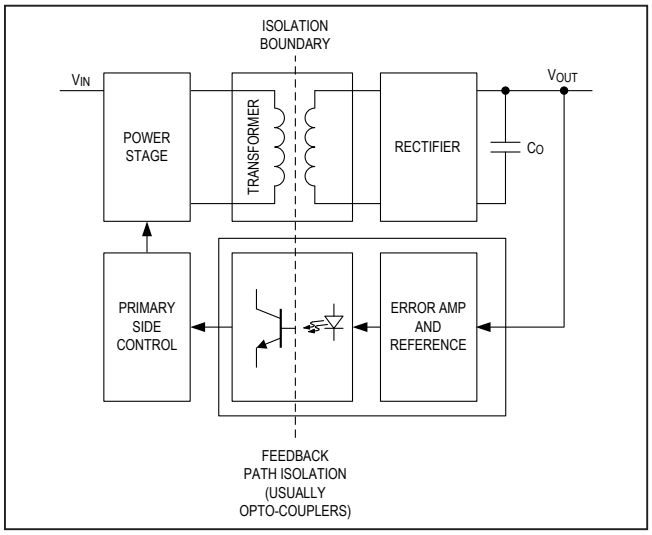

Figure 2. Generic isolated power supply.

Flyback Principle

A transformer in a flyback configuration acts differently than its usual operation of transformation of energy from primary to secondary. During a transformer's usual operation, both primary and secondary windings conduct together at the same time to make the transfer of energy possible from primary to secondary. In a flyback configuration the primary and secondary windings do not conduct at the same time and the transformer acts more like a coupled inductor. Note that in this document we have used the following notations for the transformer turns ratio:

$$K = \frac{N_P}{N_S}$$

$$k = \frac{N_S}{N_P}$$

This means capital K for primary turns/secondary turns and small k for secondary turns/primary turns.

Figure 3 shows a simple flyback topology that consists of a transformer whose primary winding is connected to the drain of a switching MOSFET. The source of the MOSFET is connected to ground. The secondary winding is connected to the output capacitor through a rectifier diode. In this flyback configuration the current flows into the primary winding during the on time of the switching period and flows into the secondary winding during the off time of the switching period.

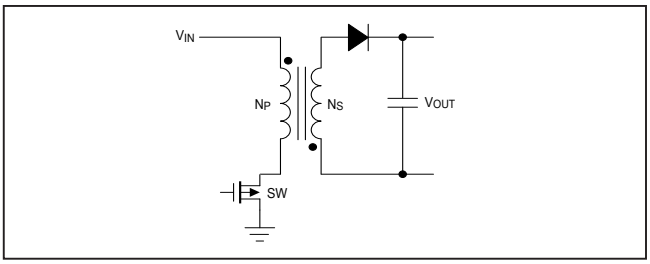

Figure 3. Simple flyback topology.

During the on-time when the primary switch is closed, a current, I_P, flows through the primary winding as shown in Figure 4. I_P can be written as follows:

$$I_P(t) = \frac{1}{L_P}\int_0^t V_{IN}d\tau = \frac{1}{L_P}V_{IN}t$$

The peak magnitude of the primary current can be written as follows:

$$I_{P-P} = \frac{1}{L_P}\int_0^{t_{ON}} V_{IN}d\tau = \frac{1}{L_P}V_{IN}t_{ON}$$

In the secondary winding, a negative voltage is induced due to the current flowing in to the primary. The rectifier diode is reverse-biased and no current is flowing in the secondary winding. The induced voltage in the primary can be written as:

$$V_S(t) = L_S \times \frac{dI_P(t)}{dt}$$

During the off-time when the primary switch opens as shown in Figure 5, the magnetic field in the primary winding collapses and the voltage at the winding reverses, while current keeps flowing in the same direction until the field fades away.

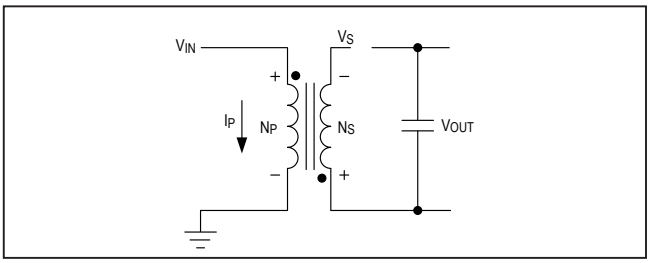

Figure 4. Flyback topology during on-time, t_{ON}.

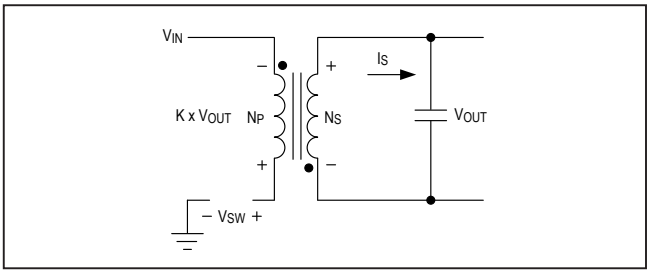

Figure 5. Flyback topology during off-time, t_{OFF}.

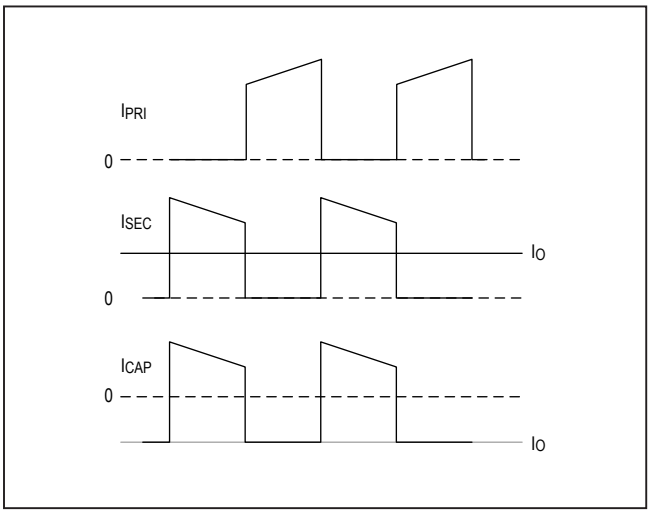

Figure 6. A typical CCM mode flyback primary and secondary winding current.

The secondary current I_S flows and the secondary and rectifier diode is forward-biased. Output voltage V_{OUT} is now available across the secondary coil if we ignore the forward voltage drop of the rectifier diode. The secondary winding voltage is now flown away to primary side as K x V_{OUT}. This voltage is present across the switch until the current in the secondary winding decays to zero. Total voltage available across the switch during the off-time can be written as:

$$V_{SW} = V_{IN} + K \times V_{OUT}$$

This voltage also causes the breakdown of the magnetic flux in the primary winding (no current is flowing in the primary winding after this reset). Here we can see that unlike a usual transformer action where current flows in both the winding at the same time, in a flyback transformer the current flows into the primary winding during the on-time and into the secondary winding during the off-time. This is why we use the term “coupled storage inductor” for transformers used in flyback operation. It should be noted though that mechanically these transformers are like any transformer. Use in flyback operations makes transformers act differently as coupled inductors. The required duty cycle for a given input voltage and output voltage can be calculated from:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

where:

$$V_{OUT} = (V_{OUT} + V_F) \times \frac{N_P}{N_S}$$

Figure 7 shows typical waveforms of a flyback converter.

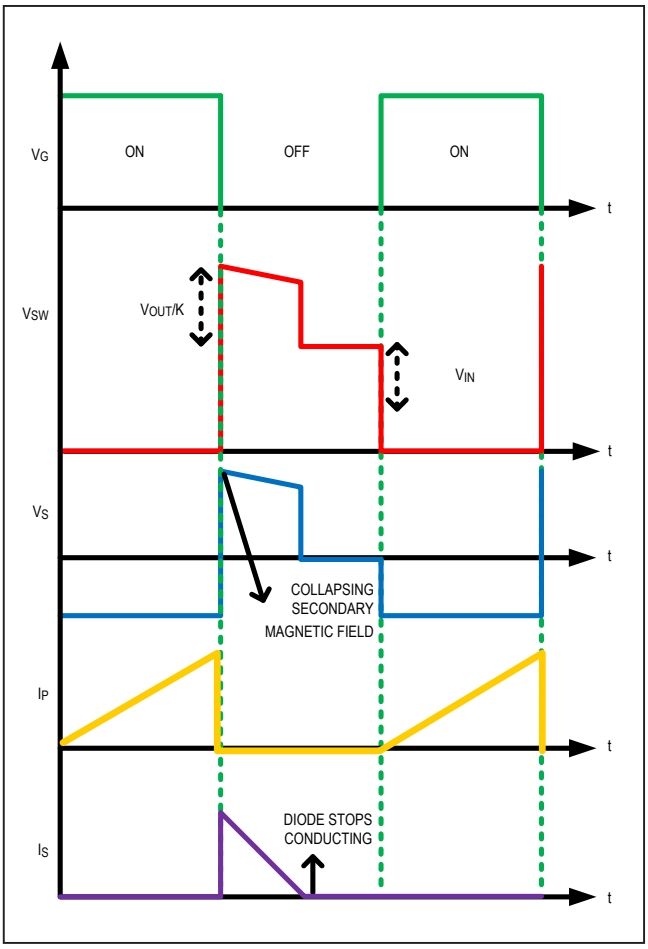

Figure 7. A typical DCM mode flyback topology waveform.

The No-Opto Flyback Converter

In isolated applications, the use of optocoupler or auxiliary winding for voltage feedback across the isolation boundary increases the number of components, and design complexity. The MAX17690 eliminates the optocoupler or auxiliary winding, and saves board space up to 30% (Figure 8). It achieves ±5% output voltage regulation over line, load, and temperature variations. The MAX17690 implements an innovative algorithm to sample and regulate the output voltage by employing primary-side sensing. Therefore, we refer to it as voltage regulation using primary-side sensing.

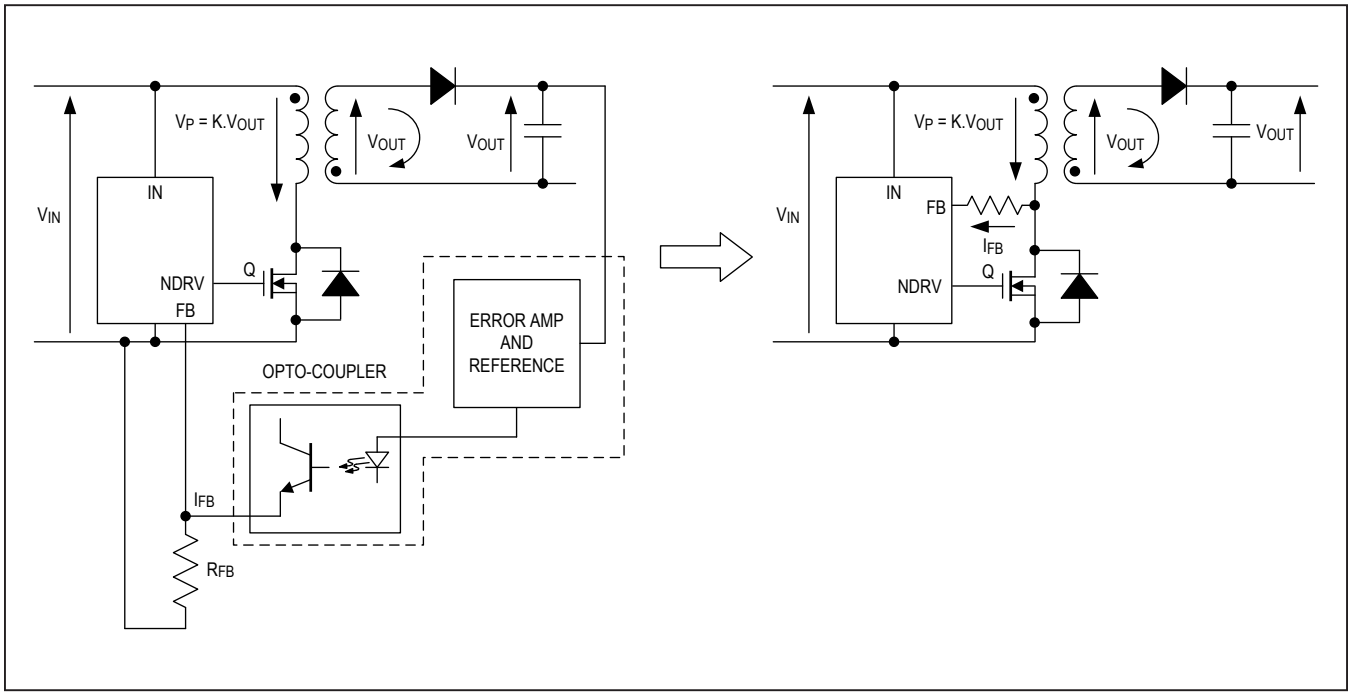

Figure 8. No-opto technology saves board area up to 30%.

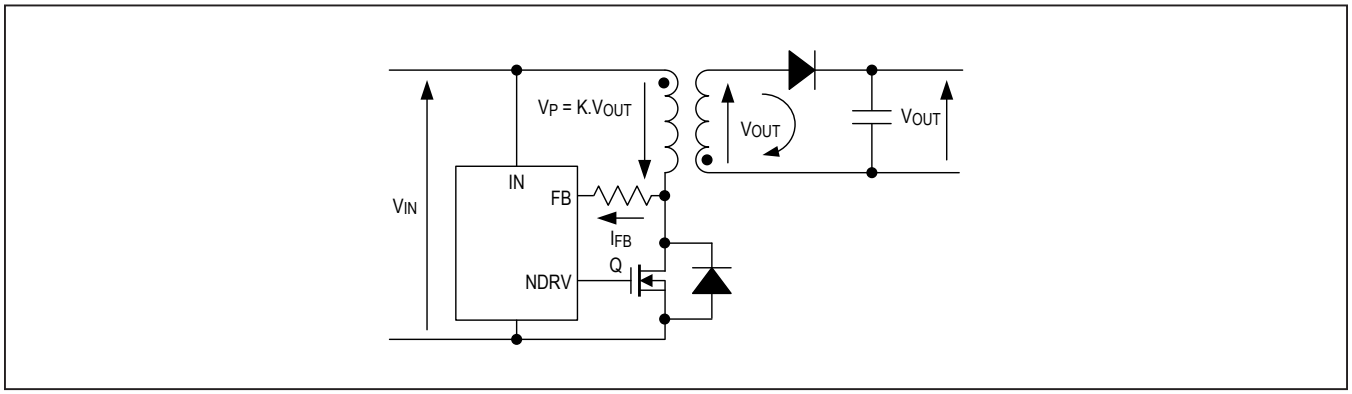

Figure 9. No-opto flyback operation eliminates the use of opto-coupler and feedback circuitry.

MAX17690 Algorithm

The MAX17690 implements an innovative algorithm to sample and regulate the output voltage by employing primary-side sensing. During the flyback period, the reflected voltage across the primary winding is the sum of output voltage, diode forward voltage, and the drop across transformer parasitic elements, multiplied by the primary-secondary turns ratio. It means that output voltage information is somewhat present at the primary coil in the form of K x V_{OUT}. The MAX17690 samples the output voltage during this time, however, the real challenge is to extract the V_{OUT} information as accurate as possible by nullifying the effects of diode voltage drop and other associated parasitics. This increases the regulation accuracy and optimize the efficiency of overall system.

The dependency of the diode's forward-voltage drop on the load current is a major cause of regulation inaccuracy. We know that the diode's forward voltage is low for low values of load current, and vice versa. Therefore, sampling the flyback voltage should be done close to the end of the diode conduction time where the diode current is low. By sampling this reflected voltage close to the secondary zero current, the algorithm minimizes the effect of transformer parasitics and the diode forward voltage on the output voltage regulation.

It is important to note that the effect of diode forward voltage is zero when the diode current is zero, and that seems to be an ideal time to sample the output voltage. However, this can be very dangerous if we miss that instant of time. If that happens, we would witness large regulation inaccuracies. Therefore, sampling should be done when secondary current is very low (but not exactly zero) to give some time margin for the sample signal to come in to effect. The MAX17690 generates a sample signal approximately 250ns before the secondary current goes to zero.

Figure 10 shows the timing diagrams of the no-opto flyback important waveforms. During T1 when the MOSFET turns on the applied voltage, V_{IN} is available across the primary winding and the primary current ramps up and flows into the magnetizing inductance L_M. This current induces a voltage in the secondary winding that reverse-biases the rectifier diode, and no current flows into the secondary winding during T1. As shown in Figure 11, instead of using a diode we have used the MAX17606 synchronous rectifier controller IC to ensure high efficiency. Figure 11 shows the state T1 when the MOSFET is on and current flows into the primary winding. A voltage is induced in the secondary winding because of the current in primary. The polarity of the induced voltage reverse biases the rectifier diode and no current flows into the secondary winding during T1.

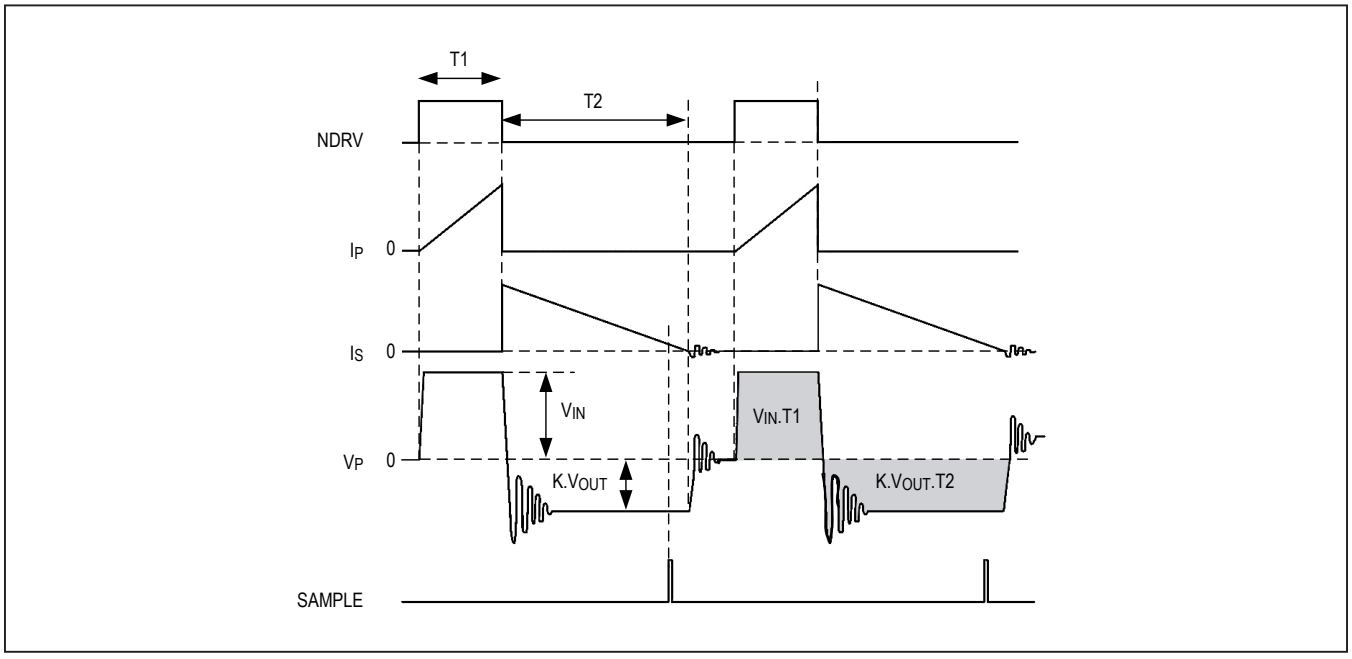

Figure 10. Timing diagram of no-opto flyback waveforms.

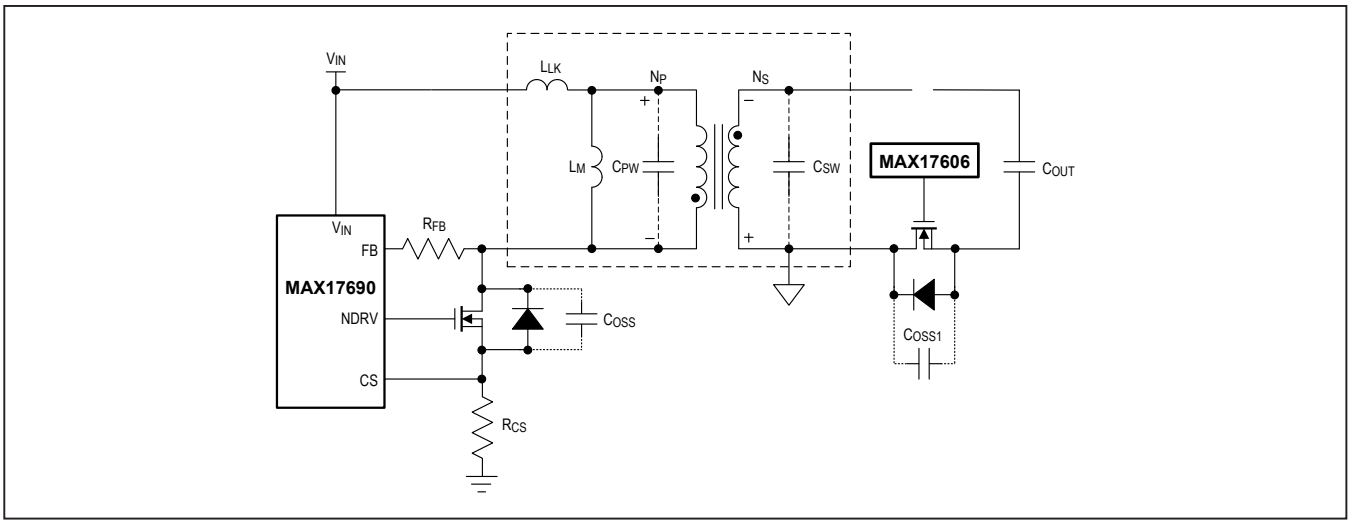

Figure 11. Circuit schematic when the MOSFET is on.

Figure 12 shows the waveforms of drain-source voltage and primary current when the MOSFET turns on. The initial ringing in the primary current rise waveform is due to the leakage inductance of the transformer and the total parasitic capacitance, C_{PAR}, which can be written as follows:

$$C_{PAR} = C_{PW} + k^2C_{SW} + k^2C_{OSS1}$$

where:

C_{PW} = Primary winding capacitance

C_{SW} = Secondary winding capacitance

C_{OSS1} = Parasitic capacitance of the secondary MOS

Figure 13 shows what happens when the MOSFET turns off during time period T2. During this state, the switch turns off, collapsing the magnetic field in the primary winding. Voltage reversal happens across transformer windings to keep current flowing in the same direction until the field fades away. The diode conducts and output voltage V_{OUT} is now available across secondary winding (ignoring diode drop). A current flows into the secondary winding, which induces a voltage across the primary winding because of the transformer action. The voltage across the MOSFET during T2 can be written as:

$$V_{DS} = V_{IN} + K \times V_{OUT}$$

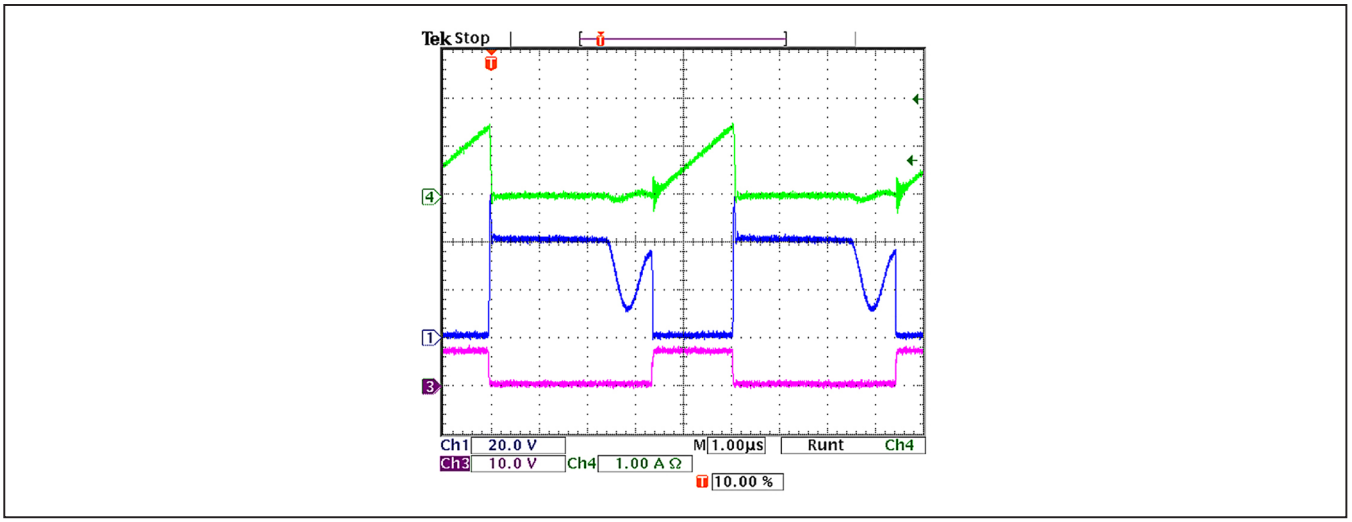

Figure 12. MOSFET is on, CH1 (blue): Primary MOSFET V_{DS}, CH3 (purple): MOSFET gate NDRV, CH4 (green): Primary current.

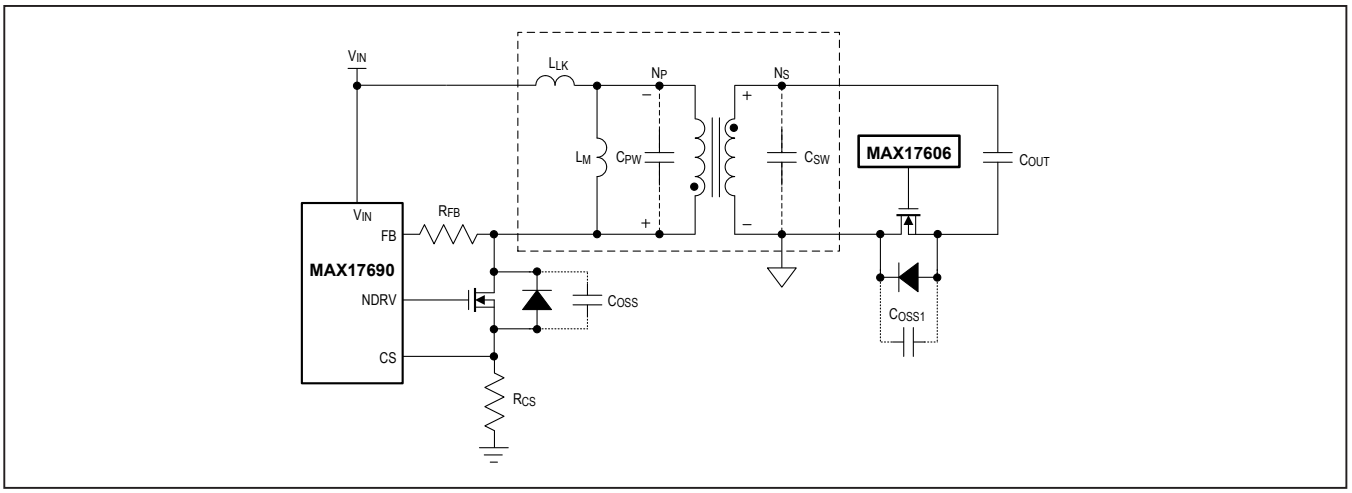

Figure 13. Circuit schematic when the MOSFET is off.

Figure 14 shows the waveforms of drain-source voltage and secondary current when the MOSFET turns off. Point 1 in Figure 14 shows the ringing drain-source voltage of the MOSFET as it turns off. This ringing is due to the leakage inductance of the transformer and the parasitic capacitance C_{PAR1}, where C_{PAR1} can be written as:

$$C_{PAR1} = C_{PW} + k^2C_{SW} + C_{OSS}$$

where:

C_{PW} = Primary winding capacitance

C_{SW} = Secondary winding capacitance

C_{OSS} = Parasitic capacitance of the primary MOS

Point 2 in Figure 14 shows the time at which the secondary current is nearly approaching zero and the reflected output voltage on the primary is sampled by the MAX17690. Point 3 in Figure 14 shows that as the current in the secondary winding ramps down to zero during the off-time, the drain-source voltage of the primary MOSFET rings from V_{IN} + (K x V_{OUT}) to V_{IN}. This ringing is due to the transformer magnetizing inductance and the associated parasitic capacitance C_{PAR2}, where C_{PAR2} can be written as:

$$C_{PAR2} = C_{PW} + k^2C_{SW} + C_{OSS} + k^2C_{OSS1}$$

where:

C_{OSS1} = Parasitic capacitance of the secondary MOS

Thus, the MAX17690 is optimized for discontinuous mode flyback operation where the stored energy in each cycle is completely delivered to the output and the primary current starts from zero in each cycle. During the time when the energy is being delivered to the output, a scaled version of the output voltage is available across the primary winding whose value is extracted by the MAX17690 intelligent algorithm. The volt-second balance expression can be written as:

$$V_{IN} \times T1 = K \times V_{OUT} \times T2$$

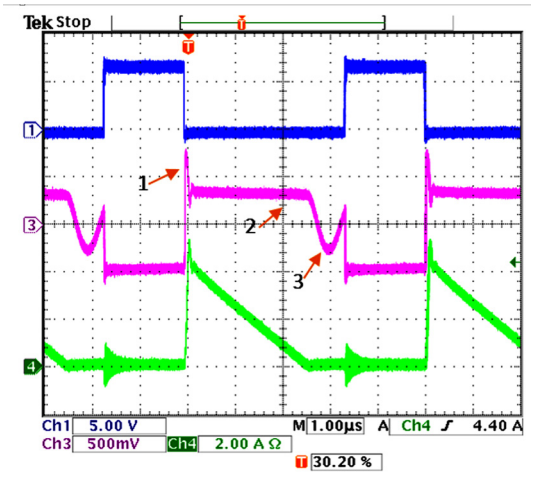

Figure 14. When the MOSFET is off, CH1 (blue): Primary MOSFET V_{DS}, CH3 (purple): MOSFET gate drive NDRV, CH4 (green): Secondary current.

Minimum Load Requirement

As previously discussed, the MAX17690 samples the reflected output voltage information on the primary winding during the time when the primary MOSFET is turned off and energy stored during the on-time is being delivered to the secondary. It is therefore mandatory for the MAX17690 to switch the external MOSFET to sample the reflected output voltage. Thus, switching is required even when there is no load requirement to keep track of the output voltage information. The current-sense voltage V_{CS} has a minimum value of 20mV, which roughly corresponds to 1/5th the full load peak current, I_{PK}. In other words, V_{CS} has a value of 100mV at full-load peak current I_{PK}. Thus, V_{CS} varies from 20mV to 100mV from minimum load to full load.

At lower output power levels that demand energy less than the minimum primary current, the MAX17690 modulates the switching frequency between $f_{SW}/4$ and f_{SW} to adjust the energy delivered to the correct level required to regulate the output voltage. As the load current is lowered further, the MAX17690 spends more and more switching cycles at $f_{SW}/4$, until the device completely settles down at $f_{SW}/4$. At this point the MAX17690 has reached its minimum load condition, and cannot regulate the output voltage without this minimum load connected to the output. This small minimum load can easily be provided on the output by connecting a fixed resistor. In the absence of a minimum load, the output voltage rises to higher values. To protect for this condition, a Zener diode of appropriate breakdown voltage rating can be installed on the output.

The maximum load power corresponds to V_{CSMAX} of 100mV. In a discontinuous flyback converter, the deliverable load current is proportional to the square of the primary peak current. V_{CSMIN} of 20mV corresponds to a 4% of full load current (for 100% efficiency) at the switching frequency of f_{SW} as follows:

At full load:

$$V_{OUT} \times I_{FULLOAD} = \frac{1}{2} \times L_{MAG} \times I_{PK}^{2} \times f_{SW}$$

At light load:

$$V_{OUT} \times I_{MINLOAD} = \frac{1}{2} \times L_{MAG} \times \left(\frac{I_{PK}}{5}\right)^{2} \times f_{SW}$$

$$V_{OUT} \times I_{MINLOAD} = \frac{V_{OUT} \times I_{FULLLOAD}}{25}$$

$$I_{MINLOAD} = 4\% \times I_{FULLLOAD}$$

Since the MAX17690 can drop its switching frequency to $f_{SW}/4$, the minimum load requirement reduces further to 1%.

$$V_{OUT} \times I_{MINLOAD} = \frac{1}{2} \times L_{MAG} \times \left(\frac{I_{PK}}{5}\right)^{2} \times \frac{f_{SW}}{4}$$

$$V_{OUT} \times I_{MINLOAD} = \frac{V_{OUT} \times I_{FULLLOAD}}{100}$$

$$I_{MINLOAD} = 1\% \times I_{FULLLOAD}$$

In practice, the efficiency is less than 100%, resulting in a minimum load requirement of less than 1%.

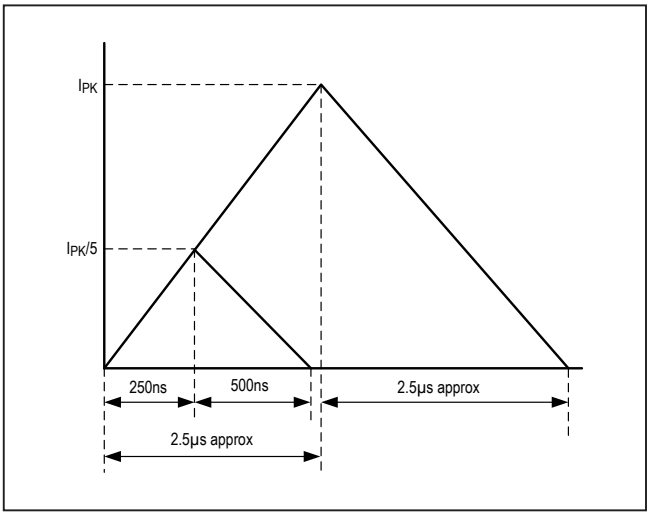

Figure 15. Peak current variation with the load.

t_{ONMIN} and t_{OFFMIN} Constraints

The MAX17690 has minimum on- and off-time constraints that set a limit on the maximum switching frequency. As previously discussed, current-sense voltage has a minimum value of 20mV at lower load currents with operating frequency of $f_{SW}/4$ and peak inductor current of $I_{PK}/5$. This 20mV must be reached within the recommended minimum on time of 230ns. A device must sample at least 250ns (minimum value in the IC data sheet is 230ns, but we give a margin and select 250ns) before the secondary current reaches zero, therefore, the recommended minimum off time is approximately 500ns in this case.

On the other hand, at higher loads with an operating frequency of f_{SW} and the peak inductor current of I_{PK}, the maximum current-sense voltage of 100mV must be reached within the recommend minimum on time of 1.25µs (5 x 250ns). The minimum off time in this case should be 2.5µs (5 x 500ns). Thus, the total time is 3.75µs, which corresponds to a maximum switching frequency of approximately 250kHz.

Design Procedure for No-Opto Flyback Using MAX17690

Now that the operation principle of the no-opto flyback is understood, a practical design can be illustrated. This document is primarily concerned with the power stage design and the feedback loop, and is intended to complement the information contained in the MAX17690 data sheet for details on how to set up supervisory and protection functions of the controller.

Step 1: Selection of Duty Cycle

Substitute the values of V_{INMIN} and V_{INMAX} from Table 1 in the formula below to calculate the maximum duty cycle D_{MAX} as follows:

$$D_{MAX} = \left(\frac{V_{INMAX}}{V_{INMAX} + (2 \times V_{INMIN})} \right)$$

$$D_{MAX} = \left(\frac{60}{60 + (2 \times 18)} \right) = 0.625$$

Step 2: Switching Frequency

The MAX17690 switching frequency is programmable between 50kHz and 250kHz with a resistor R_{RT} connected between RT and SGND. Based on the sampling algorithm requirements, for the given minimum and maximum input voltage, the maximum switching frequency is determined as follows:

$$f_{SW} \le \left(\frac{720000 \times D_{MAX} \times V_{INMIN}}{V_{INMAX}} \right)$$

$$f_{SW} \le \left(\frac{720000 \times 0.625 \times 18}{60} \right)$$

where $f_{SW} \le 135kHz$.

For this design to achieve higher efficiency, the switching frequency is selected as 125kHz. The R_{RT} is calculated for the selected f_{SW}:

$$R_{RT} = \frac{5 \times 10^6}{f_{SW}} \Omega$$

$$R_{RT} = \frac{5 \times 10^9}{125k} = 40k\Omega$$

A standard 40.2kΩ resistor is selected for R_{RT}.

Step 3: Transformer Magnetizing Inductance and Turns Ratio

Once the switching frequency and duty cycle are selected, the transformer magnetizing inductance (L_{MAG}) can be calculated from the energy balance equation given in the data sheet:

$$L_{MAG} = \frac{0.4 \times (V_{INMIN} \times D_{MAX})^2}{V_{OUT} \times I_{OUT} \times f_{SW}}$$

$$L_{MAG} = \frac{0.4 \times (18 \times 0.625)^2}{54 \times 1.1 \times 125k} = 6.818\mu H$$

For the present design L_{MAG} is chosen to be 6.8µH. The leakage inductance of the transformer should be targeted as low as possible. For this design, we have achieved leakage inductance equal to 1.7% of magnetizing inductance as follows:

$$L_{LKG} = 0.017 \text{ x } 6.8\mu = 115.6nH$$

Use the following equations to calculate the maximum duty cycle of the converter for the selected frequency and magnetizing inductance:

$$D = \frac{\sqrt{2.5 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times f_{SW}}}{V_{INMIN}}$$

$$D = \frac{\sqrt{2.5 \times 6.8\mu \times 54 \times 1.1 \times 125k}}{18} = 0.624$$

Calculate the required transformer turns ratio (k) using the below formula:

$$k = \frac{N_s}{N_p} = \frac{0.8 \times V_{OUT} \times (1 - D)}{D \times V_{INMIN}}$$

$$k = \frac{N_s}{N_p} = \frac{0.8 \times 54 \times (1 - 0.625)}{0.625 \times 18} = 1.44$$

For the present design, k is chosen as 1:1.44.

We selected the Würth Electronik transformer 750317095, which fulfills all the above mentioned required specifications for this design.

Step 4: Selection of Current-Sense Resistor

The transformer primary peak current is dependent on the output power. For the selected L_{MAG} and f_{SW}, the peak primary peak current is:

$$I_{LIM} = \sqrt{\frac{2.3 \times V_{OUT} \times I_{OUT}}{L_{MAG} \times f_{SW}}}$$

$$I_{LIM} = \sqrt{\frac{2.3 \times 54 \times 1.1}{6.8\mu \times 125k}} = 12.67A$$

The value of R_{CS} decides the peak current limit and the run-away current limit. Use the below formula to select the R_{CS}:

$$R_{CS} = \frac{0.08}{I_{LIM}} = 6.3m\Omega$$

For this application, a standard 6mΩ resistor is selected.

Step 5: Calculate the t_{ONMIN} and t_{OFFMIN}

The MAX17690 has the minimum current-sense voltage threshold limit at 20mV. For the selected current sense resistor, the minimum primary peak current allowed by the converter is:

$$I_{PRIMARY\_MIN} = \frac{0.02}{R_{CS}} = \frac{0.02}{0.006} = 3.33A$$

The minimum time required by the converter to reach the minimum primary peak current can be calculated as follows:

$$t_{ONMIN} = \frac{L_{MAG} \times I_{PRIMARY\_MIN}}{V_{INMAX}}$$

$$t_{ONMIN} = \frac{6.8\mu \times 3.33}{60} = 377.7ns$$

The calculated t_{ONMIN} 377.7ns is higher than the MAX17690 t_{ONMIN} constraint of 250ns. Similarly, the minimum off-time of the converter is calculated as:

$$t_{OFFMIN} = \frac{K \times L_{MAG} \times I_{PRIMARY\_MIN}}{V_{OUT}}$$

$$t_{OFFMIN} = \frac{1.44 \times 6.8\mu \times 3.33}{54} = 604.4ns$$

The calculated t_{OFFMIN} 604.4ns is higher than the MAX17690 t_{OFFMIN} constraint of 500ns.

Step 6: Selection of Secondary Diode

The maximum operating reverse-voltage rating must be higher than the sum of the output voltage and the reflected input voltage.

$$V_{SEC,DIODE} = 1.5 \times (k \times V_{INMAX} + V_{OUT})$$

$$V_{SEC,DIODE} = 1.5 \times (1.44 \times 60 + 54) = 210.6V$$

We used a Vishay VS-10CSH02-M3 200V, 10A diode for the secondary-side rectification. This diode has a maximum 0.98V forward voltage drop.

The secondary diode forward voltage drop (V_D) has a significant negative temperature coefficient. To compensate for this, a positive temperature coefficient current source is internally connected to the SET pin. The voltage at the TC pin is regulated to 0.55V at room temperature. This voltage has a 1.85mV/°C positive temperature coefficient. The R_{TC} resistor connected between the TC pin and SGND sets the current V_{TC}/R_{TC} into the SET pin. $\delta V_D/\delta T$ is the temperature coefficient of the selected secondary rectifier diode and its value is 1 mV/°C. Whereas, $\delta V_{TC}/\delta T$ has a value of 1.85mV/°C. Using the previous values, the R_{TC} resistor value can be calculated to be equal to 1017.132kΩ. A typical 1020kΩ resistor is selected as R_{TC}.

$$V_D = 0.98V$$

Step 7: R_{RIN}, R_{FB}, and R_{SET} Resistor Selection

Select R_{SET} = 10kΩ. R_{FB} and R_{SET} are calculated as follows:

$$R_{FB} = \left(\frac{N_P \times R_{SET}}{N_S}\right)\left((V_{OUT} + V_D) + \frac{0.55 \times (\delta V_D/\delta T)}{(\delta V_{TC}/\delta T)}\right)$$

$$R_{FB} = \left(\frac{1 \times 10k}{1.44}\right)\left((54 + 0.98) + \frac{0.55 \times 1}{1.84}\right) = 383.88k\Omega$$

Two standard resistors of values 383kΩ and 3kΩ are used in series as R_{FB}:

$$R_{FB1} = 383k\Omega$$

$$R_{FB2} = 3k\Omega$$

Note: Two series resistors are used to allow fine tuning of R_{FB} that could be required while doing hardware testing to alleviate any parasitics effect that has not been included in the above formula. The required R_{RIN} value can be calculated as follows:

$$R_{RIN} = 0.6 \times R_{FB} = 0.6 \times 386k = 231.6k\Omega$$

A standard 232kΩ resistor is selected: R_{RIN} = 232kΩ.

Step 8: Soft-Start Capacitor

For the desired soft-start time (t_{SS} = 100ms), the soft-start capacitor is selected using:

$$C_{SS} = 5 \times t_{SS} = 500nF$$

where 470nF is selected as the soft-start capacitor, C_{SS} = 470nF.

Step 9: Selection of R_{VCM} Resistor

Calculate the internal scaling factor K_C as follows:

$$K_C = \frac{100\mu \times (1 - D)}{3 \times f_{SW} \times 10^{-12}}$$

$$K_C = \frac{100 \times 10^{-6} \times (1 - 0.625)}{3 \times 125k \times 10^{-12}} = 100$$

From Table 2 choose the next higher value for the calculated K_C. For our design, the next higher value is K_C = 160. Select the resistor value corresponding to the choice of K_C as the R_{VCM}, where a standard 121kΩ resistor is selected: R_{VCM} = 121kΩ.

Table 2. R_{VCM} Resistor Selection

K_C	R_{VCM} (kΩ)
640	0
320	75
160	121
80	220
40	Open

Step 10: MOSFET Selection

The maximum voltage stress on the switching MOSFET during off-time is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating should be selected according to the result of the expression below:

$$V_{DSMAX} = V_{INMAX} + \left(\frac{2.5 \times (V_{OUT} + V_D)}{k}\right)$$

$$V_{DSMAX} = 36 + \left(\frac{2.5 \times (54 + 0.98)}{1.44}\right) = 156V$$

For this application, we selected an n-channel 200V MOSFET (IPB107N20N3 G from Infineon) as the primary MOSFET.

Step 11: Output Capacitor Selection

The output capacitance is chosen so that the output voltage has at most ±3% deviation for a 50% load step of the rated output current. The bandwidth is usually selected in the $f_{SW}/20$ to $f_{SW}/40$ range. For the present design, the bandwidth chosen is 6.25kHz. The response time $t_{RESPONSE}$ and the required output capacitance can be calculated as follows:

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

$$t_{RESPONSE} \cong \frac{0.33}{6.25k} + \frac{1}{125k} = 60.8\mu s$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$C_{OUT} = \frac{0.55 \times 60.8}{2 \times 1.62} = 10.32\mu F$$

Due to the DC-bias characteristics, a 4.7µF, 100V, 2220 capacitor offers 2.585µF at 54V. Hence, four 4.7µF, 100V, 2220 capacitors are selected for the present design.

Step 12: Loop Compensation

The MAX17690 is compensated using an external resistor capacitor network on the COMP pin. The loop compensation network are connected as shown in Figure 16. The loop compensation passive components values are calculated below. The load pole frequency is calculated as follows:

$$f_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}}$$

$$f_P = \frac{1.1}{\pi \times 54 \times 10.34\mu} = 628Hz$$

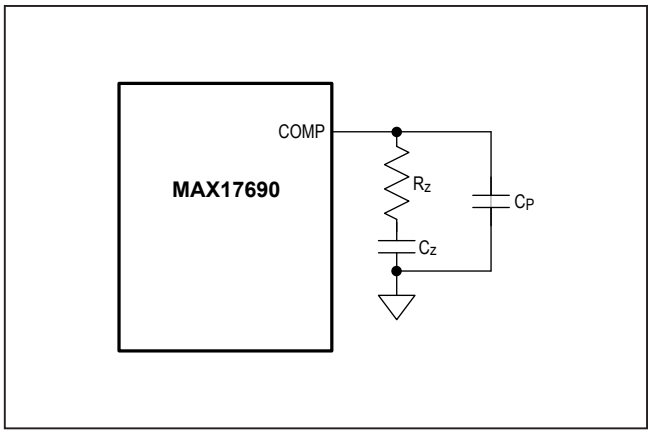

Figure 16. Loop compensation arrangement.

The compensation network components R_Z, C_Z, and C_P can be calculated as follows:

$$R_Z = 12500 \times R_{CS}\left(\frac{f_C}{f_P}\right)\sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times f_{SW}}}$$

$$R_Z = 12500 \times 6m \times \left(\frac{6.25k}{628}\right)\sqrt{\frac{54 \times 1.1}{2 \times 6.8\mu \times 125k}} = 4.41k\Omega$$

A standard 4.7kΩ is selected: R_Z = 4.7kΩ.

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P}$$

$$C_Z = \frac{1}{2\pi \times 4.7k \times 628} = 53.9nF$$

A standard 68nF capacitor is selected: C_Z = 47nF.

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

$$C_P = \frac{1}{\pi \times 4.7k \times 125k} = 677pF$$

A standard 560pF capacitor is selected: C_P = 560pF.

Step 13: EN/UNLO and OVI Setting

The EN/UVLO pin serves as an enable/disable input as well as an accurate programmable input UVLO pin. The MAX17690 does not commence startup operation until the EN/UVLO pin voltage exceeds 1.215V. The MAX17690 turns off if the EN/UVLO pin voltage falls below 1.1V. A resistor-divider from V_{IN} to SGND can be used to divide and apply a fraction of the input voltage to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.215V turn-on threshold at the desired input bus voltage. For an overvoltage input voltage specification of 37V and V_{START} of 18V, the value of R_{EN} can be calculated as follows, assuming a 10kΩ resistor for R_{OVI}.

$$R_{OVI} = 10k\Omega$$

$$R_{EN} = R_{OVI} \times \left(\frac{V_{OVI}}{V_{START}} - 1 \right)$$

$$R_{EN} = 10k \times \left(\frac{61}{18} - 1 \right) = 23.8k\Omega$$

A standard 24kΩ resistor is selected: R_{EN} = 24kΩ.

The same resistor-divider can be modified to implement input overvoltage protection. When the voltage at the OVI pin exceeds 1.215V, the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V.

$$R_{EN-TOP} = \left[R_{OVI} + R_{EN} \right] \times \left[\frac{V_{START}}{1.215} - 1 \right]$$

$$R_{EN-TOP} = \left[10k + 24k \right] \times \left[\frac{18}{1.215} - 1 \right] = 469k\Omega$$

A standard 470kΩ resistor is selected: R_{EN-TOP} = 470kΩ.

Step 14: R_{CD} Snubber Selection

Parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer and the MOSFET output capacitance, cause voltage overshoot and ringing on the MOSFET's drain node. Snubber circuits are used to limit the voltage overshoot to safe levels, within the voltage rating of the external MOSFET. Figure 18 shows the widely used R_{CD} snubber circuit. Total power dissipation in the snubber can be calculated as follows:

$$P_{SNUB} = 0.833 \times L_{LK} \times I_{LIM}^2 \times f_{SW}$$

$$P_{SNUB} = 0.833 \times 115.6n \times 12.6^2 \times 125k = 1934mW$$

The R_{SNUB} value can be calculated as follows:

$$R_{SNUB} = \frac{6.25 \times (V_{OUT} + V_D)}{K^2 \times P_{SNUB}}$$

$$R_{SNUB} = \frac{6.25 \times (54 + 0.98)}{1.44^2 \times 1934m} = 4.7k\Omega$$

A standard 4.7kΩ is selected: R_{SNUB} = 4.7kΩ.

The value of the C_{SNUB} can be calculated as follows:

$$C_{SNUB} = \frac{2 \times L_{LK} \times I_{LIM}^2 \times K^2}{(V_{OUT} + V_D)^2}$$

$$C_{SNUB} = \frac{2 \times 115.6n \times 12.6^2 \times 1.44^2}{(54 + 0.98)^2} = 22.5nF$$

A standard 22nF capacitor is selected: C_{SNUB} = 22nF.

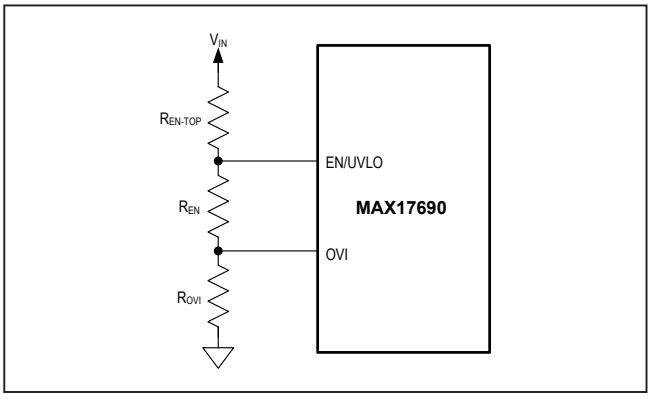

Figure 17. Programming EN/UVLO and OVI.

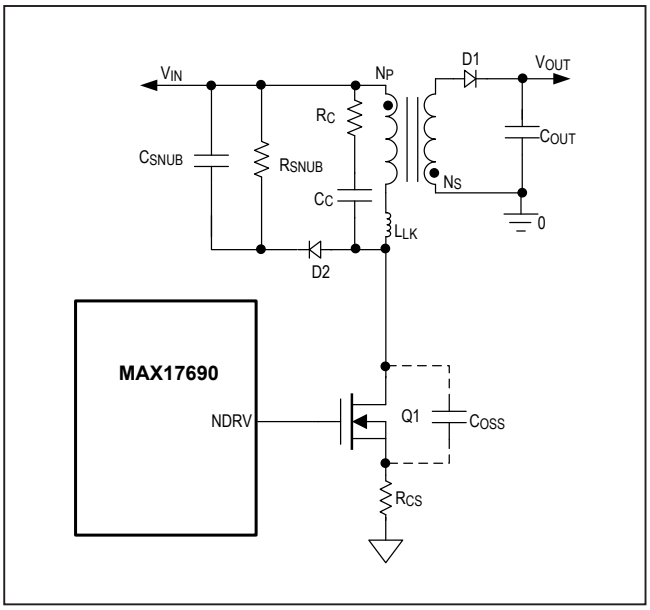

Figure 18. Snubber circuit.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/18	Initial release	—
1	3/18	In Table 1, increased the maximum efficiency from 85% to 91%.	1
2	4/18	Updated Figure 7.	3