

## Introduction

The MAX17506 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFET operates over a 4.5V to 60V input. The converter can deliver up to 5A and generates output voltages from 0.9V up to  $0.9 \times V_{IN}$ . The feedback (FB) voltage is accurate to within  $\pm 1.4\%$  over  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The MAX17506 uses peak current-mode control and can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), and discontinuous conduction mode (DCM) control schemes.

Key features include the following:

- Wide 4.5V to 60V Input
- Adjustable 0.9V to  $0.9 \times V_{IN}$  Output
- 100kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization
- 100kHz to 2.2MHz Adjustable Switching Frequency
- Up to 5A Output Current
- Fully Assembled and Tested
- Proven PCB Layout



Figure 1. MAXREFDES1054 hardware.

## Hardware Specification

This is a single-output, synchronous buck, step-down DC-DC converter design for small size and low output voltage.

Table 1 shows an overview of the design specification.

### Hardware Needed for Quick Setup

- 4.5V to 60V, 10A DC input power supply
- MAXREFDES1054# board
- Load capable of sinking 5A
- Digital voltmeter (DVM)

### Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	$V_{IN}$	10V	55V
Frequency	$f_{SW}$	300kHz	
Efficiency	$\eta$	95%	
Output Voltage	$V_{OUT}$	4V	
Output Voltage Ripple	$\Delta V_{OUT}$	40mV	
Output Current	$I_{OUT}$	0A	5A
Output Power	$P_{OUT}$	20W	

## Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide for the design of buck converter using the MAX17506 for low voltage and smaller size. Refer to the MAX17506 IC data sheet and MAX17506A EV kit data sheet for device operation details. The converter design has been built and tested, details of which follow later in this document.

## Buck Converter Operation

The buck power converter is a DC-DC converter whose output voltage is less than the input voltage. This is a non-isolated topology, which means the input and output share a common ground. Figure 2 shows the basic circuit of the synchronous buck power converter. The difference between synchronous buck and traditional buck is that, in a synchronous buck, a transistor NL is placed in parallel to the diode to reduce the voltage drop and, therefore, to increase the efficiency.

A buck power converter has the following components:

- Input capacitor ( $C_{IN}$ ) and output capacitor ( $C_{OUT}$ )
- A switch, in this case a transistor NH
- An energy storage element, inductor (L)
- Transistor NL and diode D1 to conduct during the off-state of the switch

Figure 3 shows the basic operation of the buck power converter. During the on-state ( $t_{ON}$ ) of the transistor NH, the voltage at the node LX is equal to  $V_{IN}$  and then the current across the inductor rises linearly at a rate of  $(V_{IN} - V_{OUT})/L$ . When the transistor NH is off ( $t_{OFF}$ ), the voltage at the LX node is 0V and the current in the inductor falls linearly. It is the property of the inductor to maintain the flow of the current, so this reverses the polarity of the inductor during the NH off-state). The current through the inductor never falls to zero. This is called Continuous Conduction Mode (CCM). The ripple current  $\Delta I$  is an important parameter that is approximately 20 to 50 percent of  $I_L$  (load current).

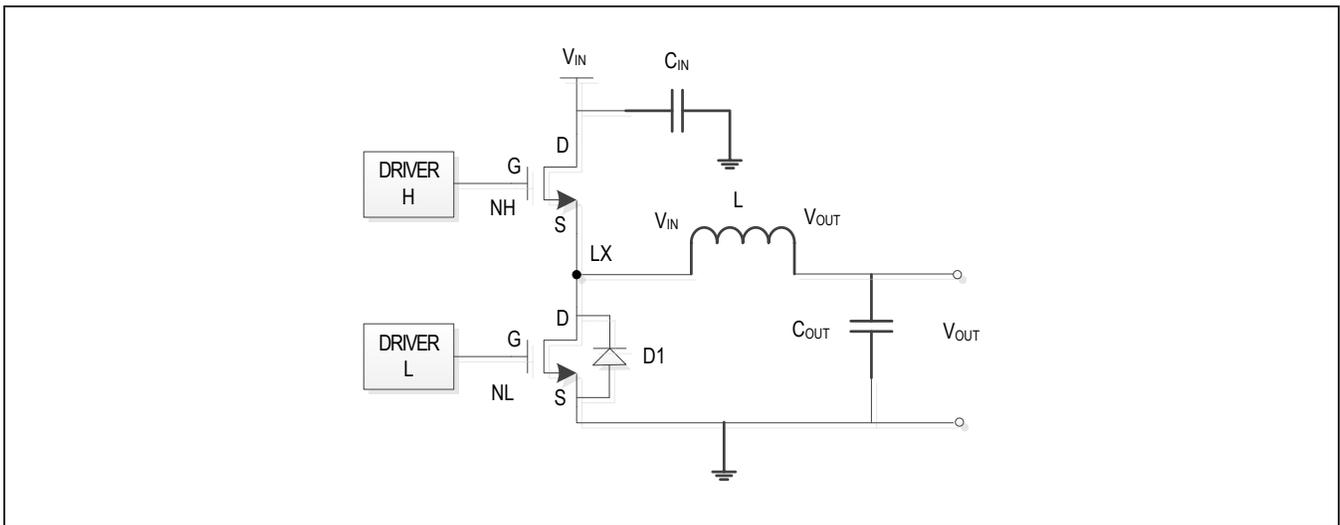


Figure 2. Synchronous buck converter.

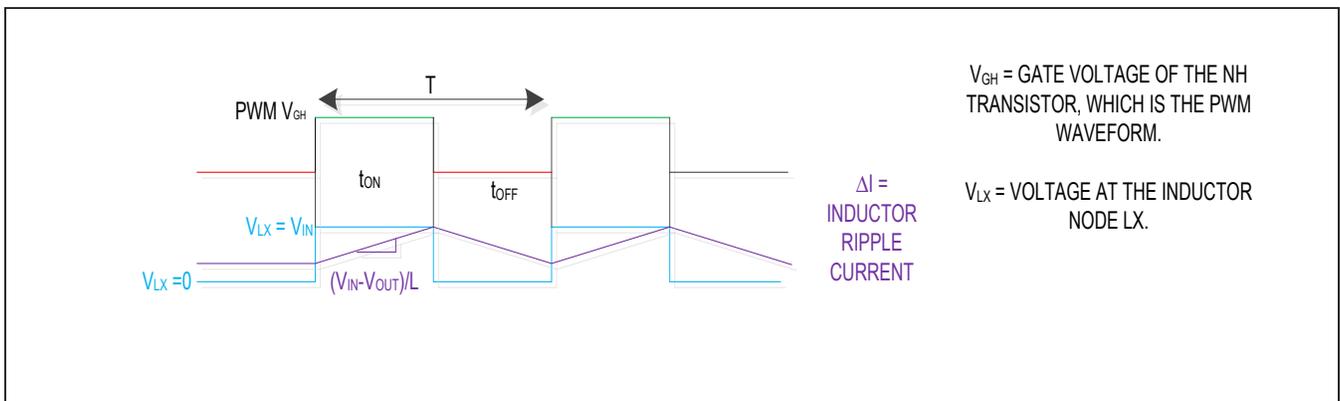


Figure 3. Basic timing waveform showing the PWM voltage and the voltage and current at the LX node.

## Design Procedure for Step-Down DC-DC Converter Using MAX17506

The theory behind the synchronous buck is explained in the previous section, so now a practical design technique is illustrated. This involves the following stages: output voltage selection, inductor and capacitor selection, and setup of the switching frequency. This document is intended to complement the information contained in the MAX17506 IC data sheet.

The following design parameters are used throughout this document:

SYMBOL	FUNCTION
$V_{IN}$	Input voltage
$V_{FB}$	Feedback threshold voltage
$V_{OUT}$	Output voltage
$\Delta V_{OUT}$	Output ripple voltage
$I_{OUT}$	Output current
$\eta$	Target minimum efficiency
$P_{IN}$	Input power
$f_{SW}$	Switching frequency
D	Duty cycle

### Step 1: Setting the Output Voltage

The MAX17506's output voltage can be adjusted between 0.9V and  $0.9 \times V_{IN}$ . The output using the R3 and R4 resistors connected to the FB pin is calculated as follows:

$$R3 = \frac{451 \times 10^3}{f_C \times C_{OUT}}$$

$$R3 = \frac{451 \times 10^3}{\left(\frac{300k}{9}\right) \times 137}$$

where R3 = 98kΩ. A 121kΩ nominal value is chosen for this design.

$$R4 = \frac{R3 \times 0.9}{V_{OUT} - 0.9}$$

$$R4 = \frac{121 \times 0.9}{4 - 0.9}$$

where R4 = 35kΩ. A 34.8kΩ nominal value is chosen for this design.

### Step 2: Setting the Switching Frequency

The MAX17506 can operate between 100kHz and 2.2MHz. The RT pin is used to set the regulator's switching frequency ( $f_{SW}$ ). RT is connected to 61.9kΩ, which gives 300kHz. This is calculated using the following equation:

$$R_{RT} = \frac{19 \times 10^3}{f_{SW}} - 1.7$$

where  $R_{RT}$  is in kΩ and  $f_{SW}$  is in kHz.

The switching frequency  $f_{SW} = 300$ kHz and  $R_{RT} = 61.33$ kΩ, so 61.9kΩ is chosen here.

### Step 3: Selecting the Output Inductor

The LX pin is connected to the switching node of the inductor. The value of the inductor is calculated as follows:

$$L = \frac{V_{OUT}}{2.2 \times f_{SW}}$$

where  $V_{OUT} = 4$ V,  $f_{SW} = 300$ kHz, and  $L = 6.06$ μH. A 5.6μH value is chosen for this design.

### Step 4: Selecting the Output and Soft-Start Capacitor

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. A capacitor connected from SS to SGND determines the soft-start. This soft capacitor depends upon the output capacitor. The output capacitance can be calculated as follows:

$$C_{OUT} = \left(\frac{1}{2} \times \left(\frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}\right)\right)$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where  $I_{STEP}$  is the load current step,  $t_{RESPONSE}$  is the response time of the controller,  $\Delta V_{OUT}$  is the allowable output voltage deviation,  $f_C$  is the target closed-loop crossover frequency, and  $f_{SW}$  is the switching frequency. Choose  $f_C$  to be 1/9th of  $f_{SW}$  because in this design the switching frequency is less than 450kHz (refer to the MAX17506 data sheet for more information).

Substitute the following values in the above equations:

$$I_{STEP} = 2.5A$$

$$\Delta V_{OUT} = 0.12V$$

$$f_C = (300k/9)$$

$$f_{SW} = 300kHz$$

$$t_{RESPONSE} = 13.2\mu s$$

$$C_{OUT} = 137.8\mu F$$

Hence, the 47µF capacitors are selected in parallel for the nominal value.

The soft-start capacitance ( $C_{SS}$ ) is calculated as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{OUT} \times V_{OUT}$$

$C_{OUT}$  is the selected output capacitance:

$$C_{SS} \geq 28 \times 10^{-6} \times 137 \times 10^{-6} \times 4$$

$$C_{SS} \geq 28 \times 10^{-6} \times 137.8 \times 10^{-6} \times 4$$

where  $C_{SS} \geq 15.43\text{nF}$ .  $C_{SS} = 47\text{nF}$  is considered the nominal value.

### Step 5: Selecting the Undervoltage Lockout (UVLO)

UVLO is a technique used to shut down the power to the IC when the input voltage is less than the operational value. R1 and R2 are used to set the UVLO of the converter. Choose R1 to be 3.3MΩ and calculate R2 as follows, with  $V_{INU} = 5.9\text{V}$ .

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

$$R2 = \frac{3.3 \times 10^6 \times 1.215}{(5.9 - 1.215)}$$

where  $R2 = 855816.44$ . A 866kΩ value is chosen in this design.

### Step 6: Compensation

The MAX17506 is internally compensated. However, if the switching frequency is less than 450kHz, a capacitor needs to be connected between the CF and FB pins. Since this design uses 300kHz, a 1pF capacitor is connected between the CF and FB pins.

### Step 7: Choosing the Mode Selection

The MODE/SYNC pin configures the MAX17506 to operate either in PWM/PFM or DCM modes. This configuration is user-flexible through jumper 2 (JU2), as defined in Table 2.

**Table 2. MODE Description (JU2)**

SHUNT POSITION	MODE PIN	MAX17506 OPERATION MODE
Not installed	Unconnected	PFM Mode
1-2	Connected to SGND	PWM Mode
2-3	Connected to VCC	DCM Mode

### Step 8: Input Capacitor Selector

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement ( $I_{RMS}$ ) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Substituting the values:

$$I_{OUT(MAX)} = 5\text{A}$$

$$V_{IN} = 24\text{V}$$

$$V_{OUT} = 4\text{V}$$

$$I_{RMS} = 1.62\text{A}$$

where  $I_{OUT(MAX)}$  is the maximum load current.  $I_{RMS}$  has a maximum value when the input voltage equals twice the output voltage ( $V_{IN} = 2 \times V_{OUT}$ ), so  $I_{RMS(MAX)} = I_{OUT(MAX)}/2\text{A}$ .

Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

Substituting the values:

$$I_{OUT(MAX)} = 5\text{A}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

$$D = \frac{4}{24} = 0.1666$$

$$\eta = 95\%$$

$$f_{SW} = 300\text{kHz}$$

$$\Delta V_{IN} = 0.5$$

where the input capacitor = 4.8µF.

### Design Resources

Download the complete set of [Design Resources](#) including the schematics, bill of materials, PCB layout, and test files.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—

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