

## Introduction

The MAXREFDES1034 is an auxiliary power supply for TV applications. This design provides a 5V output and up to 5A of load current for system power of auxiliary functions such as monitoring and control. A wide operating range from 11.5V to 28V allows system designers to adapt this design to their input voltage needs. As with most modern TVs, flat panel screens limit the available area for the converter. This power supply is a low-profile design, which considers modern TV sizes and available space. This design focuses on providing high efficiency while limiting the total height to 6mm.

This design is centered around the MAX17506 peak current-mode controller. The design is tested at 12V and 24V, which are common TV system voltages.

Other features include the following:

- Low-Profile Design (6mm Height)
- 5V/5A Output
- Built-In Soft-Start
- 300kHz Switching Frequency
- PWM Mode
- Bootstrap LDO for Improved Efficiency at High  $V_{IN}$
- Built-In Soft-Start
- Internally Compensated

## Hardware Specification

In this document a step-down DC-DC converter using the MAX17506 is demonstrated for a 5V output application. The power supply delivers up to 5A at 5V. Table 1 shows an overview of the design specification.

**Table 1. Design Specification**

PARAMETER	SYMBOL	MIN	MAX
Output Voltage	$V_{OUT}$	4.95V	5.05V
Input Voltage	$V_{IN}$	11.5V	28V
Output Current	$I_{OUT}$	0A	5A
Output Power	$P_{OUT}$		25W
Output Ripple	$\Delta V_{OUT}$		50mV
Input Ripple	$\Delta V_{IN}$		480mV
Transient Undershoot	$V_{US}$		250mV
Transient Overshoot	$V_{OS}$		250mV

## Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a step-down (buck) DC-DC converter using Maxim's MAX17506 current-mode controller. The power supply has been built and tested. Design details follow later in this document.

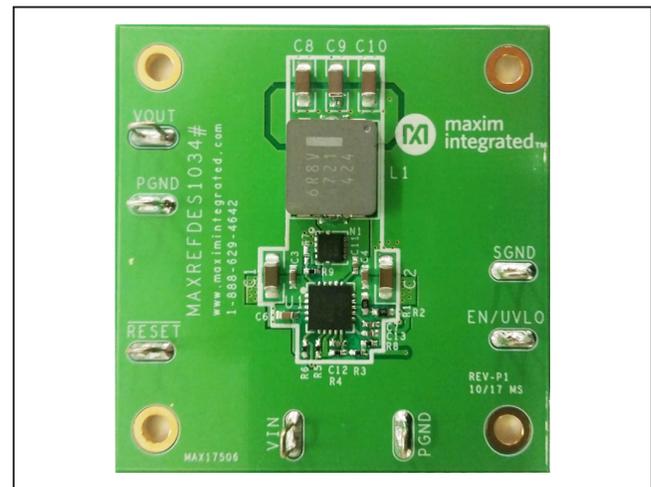


Figure 1. MAXREFDES1034 hardware.

## Design Procedure for High-Efficiency TV Power Supply Using MAX17506

The converter design process can be divided into three parts: the power stage, configuring the MAX17506 current-mode controller, and closing the control loop. A step-by-step procedure is shown to describe the design process and justify design decisions. This document is intended to complement the information contained in the MAX17506 data sheet.

The following design parameters and associated symbols are used throughout this document:

SYMBOL	FUNCTION
$V_{IN}$	Input voltage
$V_{FB}$	Feedback threshold
$V_{OUT}$	Output voltage
$\Delta V_{OUT}$	Output ripple voltage
$I_{OUT}$	Output current
$f_{SW}$	Switching frequency
D	Duty cycle

### Step 1: Choosing an Operating Mode

The MAX17506 features three operation modes: pulse-frequency modulation (PFM) mode, discontinuous conduction mode (DCM), and pulse-width modulation (PWM) mode. The PFM operation mode provides high efficiency at light loads by skipping pulses, but results in large output ripple that is dependent on load current. The DCM operation shows improved efficiency over a wider range and provides fixed-frequency operation. The PWM operation mode provides the highest efficiency at heavy loads. For more information about these operation modes, refer to the MAX17506 IC data sheet.

The MAXREFDES1034 is expected to supply up to 5A. Therefore, it is desirable to use the PWM operation mode to ensure highest efficiency and low output voltage ripple. To enable PWM mode, the MODE/SYNC pin on the MAX17506 is connected to SGND.

### Step 2: Choosing a Suitable Switching Frequency

The switching frequency can be selected based on several design criteria such as converter size, efficiency, electromagnetic interference (EMI), or electromagnetic compatibility (EMC). The MAXREFDES1034 does not have any EMI or EMC specifications, so the switching frequency is chosen by optimizing efficiency and size.

Generally, a higher switching frequency results in smaller energy storage devices (i.e., output inductor and capacitor); however, a higher switching frequency also increases switching losses and reduces overall efficiency. At lower switching frequencies, losses are mainly due to conduction of the FET's on-resistance ( $R_{DS(ON)}$ ) and output induc-

tor series resistance ( $R_{DCR}$ ), which are typically less than the switching losses. A lower switching frequency allows for higher overall efficiency, but results in larger energy storage devices.

The MAX17506 switching frequency can be programmed from 100kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. Per the MAX17506 data sheet, the switching frequency ( $f_{SW}$ ) is related to the resistor connected at the RT pin ( $R_{RT}$ ) by the following equation:

$$R_{RT} \cong \frac{19 \times 10^3}{f_{SW}} - 1.7$$

Using the above equation, we calculate the frequency setting resistor, where  $R_{RT}$  is in k $\Omega$  and  $f_{SW}$  is in kHz. For this design, a 61.9k $\Omega$  resistor was used for  $R_{RT}$  to obtain approximately 300kHz switching frequency, which permits high-efficiency operation.

### Step 3: Choosing the Input Capacitor

The input current of the buck regulator is inherently discontinuous. This discontinuous input current demands AC from the source and, hence, adds additional losses. A shunt input capacitor is used to filter the AC. The input capacitor is selected based on the maximum input voltage, allowable input voltage ripple, and the RMS current imposed on the capacitor. Below are the equations used for calculating the RMS current through the capacitor and required capacitance. The worst-case RMS current occurs when  $V_{IN} = 2 \times V_{OUT}$ , which is what we assume to obtain a worst-case estimate for RMS current. The maximum duty cycle occurs when the input voltage is at a minimum. The maximum duty cycle is used to determine the input capacitance. To determine the input capacitance, we must estimate the expected efficiency. Using the MAX17506 data sheet efficiency curves, we expect a minimum 92% efficiency.

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} = 5A \times \frac{\sqrt{5V \times (10V - 5V)}}{10V} = 2.5A$$

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(MIN)}} = \frac{5V}{11.5V} = 0.435$$

$$C_{IN} = \frac{I_{OUT(MAX)} \times D_{MAX} \times (1 - D_{MAX})}{\eta \times f_{SW} \times \Delta V_{IN}} = \frac{5A \times 0.435 \times (1 - 0.435)}{92\% \times 300kHz \times 480mV} = 9.27\mu F$$

The input capacitor must be able to withstand the maximum input voltage; thus, we select a 50V rated capacitor, which is well beyond the maximum input voltage. In addition, we must ensure the RMS ripple through the capacitor does not cause any significant heating. As a rule of thumb, we limit the capacitor to a maximum 10°C rise in temperature based on the ripple current. To achieve this, we use two 4.7 $\mu F$  ceramic capacitors

(UMK316AB7475ML) in parallel. This reduces the ripple requirement on each capacitor by half since they are in parallel (e.g.,  $1.25A_{RMS}$  per capacitor). Based on the capacitor data sheet, each capacitor produces approximately a  $3^{\circ}C$  rise in temperature for an RMS current of 1.25A, which is within our specification.

Additionally, we place two small 0.1 $\mu$ F capacitors close to the IC to reduce the effects of trace impedance. These capacitors also see the full input voltage, so they must be rated for 50V.

In applications where the source is located distant from the MAX17506, an electrolytic capacitor should be added in parallel to the ceramic capacitor. Doing so provides necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

#### Step 4: Choosing the Inductor

A high-valued inductor results in reduced inductor-ripple current, leading to a reduced output-ripple voltage. However, a large inductance requires a larger physical size or higher DCR with a lower saturation current rating. The inductor is chosen based on the IC data sheet equation as follows:

$$L = \frac{V_{OUT}}{2.2 \times f_{SW}} = \frac{5V}{2.2 \times 300kHz} = 7.58\mu H$$

We select a 6.8 $\mu$ H inductance, which is approximately 10% less than the calculated value. This inductance allows for a smaller inductor and faster transient response. The next important parameter to consider is the inductor saturation current. The inductor saturation current must be higher than the peak current in the inductor. First, we calculate the ripple current in the inductor. Then, we derive the peak current based on the average current through the inductor, which is equivalent to the average load current. To calculate the peak inductor current, the following equations are used:

$$\Delta I_{L(P-P)} = \frac{(V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} = \frac{(28V - 5V) \times \frac{5V}{28V}}{6.8\mu H \times 300kHz} = 2.01A$$

Moreover, the inductor peak current is given by:

$$I_{PK} = I_{OUT} + \frac{1}{2} \Delta I_{L(P-P)} = 5A + \frac{1}{2}(2.01A) = 6.01A$$

In addition to these calculated parameters, we must also choose an inductor with low DCR and a maximum 4mm seated height. A low DCR must be selected per the IC data sheet recommendations to provide high efficiency and fast transient response. The maximum 6mm seated height results in a low-profile design for size-constrained applications, such as power supplies in modern flat-screen TVs. This design uses a 4-layer board with a 2mm thickness, so we must ensure the height of our inductor is 4mm or less.

Considering these previously derived parameters, we select the ETQP4M6R8KVC low-profile inductor with the following specifications:

PARAMETER	VALUE
L	6.8 $\mu$ H $\pm$ 20%
DCR	20.35m $\Omega$ (max)
$I_{SAT}$	12.1A
Height	4mm

#### Step 5: Choosing the Output Capacitor

The output capacitor is selected based on either a ripple voltage or a load transient requirement. This design focuses on maintaining the output voltage within 5% upon a 0A to 2.5A load transition. The IC data sheet equations for calculating the output capacitance based on a load transient are shown below:

$$t_{RESPONSE} \cong \left( \frac{0.33}{f_C} + \frac{1}{f_{SW}} \right) = \left( \frac{0.33}{(300kHz/9)} + \frac{1}{300kHz} \right) \approx 13.2\mu s$$

$$C_{OUT} = \frac{1I_{STEP} \times t_{RESPONSE}}{2 \Delta V_{OUT}} = \frac{12.5A \times 13.2\mu s}{2 \times 250mV} = 66\mu F$$

Based on the parameter used, the resulting controller response time ( $t_{RESPONSE}$ ) is 13.2 $\mu$ s and the output capacitance is calculated to be 66 $\mu$ F. The voltage rating of the capacitor must be greater than the output voltage, so we select a 10V rated ceramic capacitor. We must also allow for a  $\pm$ 10% capacitor tolerance and a further reduction of 20% capacitance due to the DC bias effect (i.e., operating a 10V ceramic capacitor at 5V), so our final nominal value is:

$$C_{OUT} = \frac{66\mu F}{90\% \times 80\%} \approx 91.7\mu F$$

We achieve this by placing three 33 $\mu$ F capacitors (TDK C3216X5R1A336M160AB) in parallel.

#### Step 6: Choosing the Low-Side Switch

The low-side switch must be an nFET type to ensure proper operation. The switch is chosen based on the rated voltage, rated current, and on-resistance. The rated voltage is simple, since the maximum voltage the nFET sees is equivalent to the supply voltage. Thus, we must select an nFET with  $V_{DS(MAX)} > V_{IN(MAX)}$ . The peak current in the low-side switch is equivalent to the peak current in the inductor, which was previously calculated to be 6.01A. We must select an nFET with a peak current rating above 6.01A. Finally, we select the  $R_{DS(ON)}$  to be as low as possible.

Based on the requirements above, we select the Vishay SiS406DN with the following specifications:

PARAMETER	VALUE
$V_{DS}$	30V
$I_D$	12.2A at $V_{GS} = 4.5V$
$R_{DS(ON)}$	14.5m $\Omega$ at $V_{GS} = 4.5V$
$P_{MAX}$	1W at $T_A = +70^{\circ}C$

We must ensure the power dissipated in the low-side switch does not violate its maximum power dissipation. To do so, we use the following equation to determine the power dissipated in the low-side switch based on maximum load current,  $R_{DS(ON)}$ , and minimum duty cycle. The duty cycle for a buck converter is simply the ratio of the output voltage to input voltage. The minimum duty cycle occurs at maximum input voltage.

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(MAX)}} = \frac{5V}{28V} = 0.179$$

$$P_{LSFET} = I_{LOAD(MAX)}^2 \times R_{DS(ON)} \times (1 - D_{MIN})$$

$$= (5A)^2 \times (14.5m\Omega) \times (1 - 0.179) \approx 300mW$$

The power dissipation in the low-side switch is calculated to be approximately 300mW, which is far less than the nFET power rating. Thus, we conclude this device will work under the designed operating conditions.

Last, we place a small series resistor at the nFET's gate to limit the nFET's slew rate. By limiting the nFET's slew rate, we reduce the potential for switch-node ringing, voltage spikes, and EMI. A small 4.7 $\Omega$  series resistor is used but can be increased if greater EMI suppression is required. However, using too large of a resistor significantly slows the transition and causes cross-conduction. Thus, it is best to start with a low value series resistor and increase resistance to achieve the desired performance.

### Step 7: Setting the Output Voltage

The output voltage is determined by the voltage divider in the feedback loop, which consists of resistors R3 and R4. These resistor values are calculated using the following IC data sheet equations:

$$R3 = \frac{451 \times 10^3}{f_C \times C_{OUT}} = \frac{451 \times 10^3}{(300kHz / 9) \times (99\mu F)} = 136.67k\Omega$$

Thus, we select R3 = 137k $\Omega$   $\pm$ 1%, which is connected from  $V_{OUT}$  to FB.

Next, we calculate resistor R4, which is connected from FB to SGND:

$$R4 = \frac{0.9 \times R3}{(V_{OUT} - 0.9)} = \frac{0.9 \times 137k\Omega}{(5V - 0.9)} = 30.07k\Omega$$

Thus, we select R4 = 30k $\Omega$   $\pm$ 1%.

### Step 8: Choosing the Soft-Start Capacitor

Soft-start limits the inrush current by slowly ramping up the output voltage. A longer soft-start time reduces the charging rate of the output capacitor, thereby limiting the inrush current. The required soft-start time is dependent on the output voltage and output capacitance. We must ensure the selected soft-start time does not cause any harmful inrush currents; thus, the MAX17506 data sheet provides a simple equation to ensure the soft-start time is long enough to limit the inrush current to an acceptable level.

$$C_{SS} \geq 28 \times 10^{-6} \times C_{OUT} \times V_{OUT}$$

$$\geq 28 \times 10^{-6} \times 99\mu F \times 5V \geq 13.86\mu F$$

Based on this equation, we must select  $C_{SS}$  to be greater than 13.86 $\mu$ F. For this design, we select a  $C_{SS}$  = 22nF, which produces an approximately 4ms soft-start time.

### Step 9: Setting Up Bootstrap Operation

The MAX17506 internal electronics are powered by either the  $V_{CC}$  pin or the EXT $V_{CC}$  pin. The  $V_{CC}$  input uses a high-voltage LDO to regulate the input voltage to a lower system voltage, which is very inefficient when the input voltage is very large. Higher efficiencies can be achieved by using the buck output as input to a lower voltage LDO. To take advantage of this unique feature, we simply connect the buck output to the EXT $V_{CC}$  pin. An RC filter is added between the buck output and the EXT $V_{CC}$  input to increase PSRR.

We begin by selecting the filter's series resistance. The minimum operating voltage of the low-voltage LDO is 4.84V minimum; thus, we must ensure that the voltage drop across the series resistor does not cause an under-voltage condition. To ensure this does not occur, we assume a worst-case 2mA operating current. This 2mA of operating current should not cause more than 10mV drop across the series resistor. The following equation is used to estimate the size of the series resistor:

$$R_S = \frac{\Delta V_{RS}}{I_{Q(MAX)}} = \frac{10mV}{2mA} = 5\Omega$$

Thus, we select  $R_S$  = 4.7 $\Omega$ .

Finally, we select the filter capacitor to achieve a 3dB attenuation of the fundamental switching frequency. A 3dB attenuation occurs at the RC filters pole; therefore, we use the following equation to select the shunt filter capacitor:

$$C_S = \frac{1}{2\pi f_{sw} R_S} = \frac{1}{2\pi \times (300kHz) \times (4.7\Omega)} = 0.11\mu F$$

Thus, we select  $C_S$  = 0.1 $\mu$ F.

### Step 10: Setting the UVLO

UVLO turns the converter off when the input voltage is below a set threshold. The following equations are used to find the resistor-divider values that produce an 11.5V input threshold.

$R1 = 3.3M\Omega$ , per the data sheet recommendations.

Thus, we select  $R1 = 3.32M\Omega \pm 1\%$  standard value resistor.

The input voltage threshold is reduced by 2% to account for resistor tolerances. This ensures the UVLO only asserts below 11.5V.

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)} = \frac{3.32M\Omega \times 1.215}{(11.5V \times 98\% - 1.215)} = 401.17k\Omega$$

Thus, we select  $R2 = 402k\Omega \pm 1\%$  standard value resistor.

### Step 11: Choosing the BST Capacitor

An external flying capacitor is used by the MAX17506's internal electronics. This flying capacitor provides power for the internal high-side driver circuitry. Connect a  $0.1\mu F$  capacitor between BST and LX. A ceramic capacitor with a 16V rating or greater is recommended.

### Step 12: Choosing the Compensation Capacitor

The MAX17506 is internally compensated; however, since the switching frequency is less than 450kHz, we must connect a  $2.2pF$  capacitor between the CF pin and the FB pin. CF and FB are low-voltage pins used by the internal control loop; thus, we select a 10V rated ceramic capacitor.

### Design Resources

Download the complete set of [Design Resources](#) including the schematics, bill of materials, PCB layout, and test files.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/18	Initial release	—

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