How to Extend the Run-Time of Your DSLR/DSLM Camera Design

The sale of digital cameras for the professional market continues to grow at a healthy rate. Although smartphone cameras come close to matching their performance, they fail to meet the most challenging demands. Digital single lens reflex (DSLR, Figure 1) and mirrorless (DSLM) cameras have several advantages over smartphone cameras. The larger DSLR/DSLM sensors allow for larger pixels, which yield better sensitivity to light (ISO). A greater number of pixels can be packed into the larger sensors, yielding better total resolution, which translates into more detail. Additional features such as customizable lenses, true optical control of the depth of field (as opposed to software control), true optical variable aperture options, and precise control of shutter speed and ISO all help to deliver near perfect photos. Not surprisingly, higher performance comes with a cost in terms of energy drawn from the lithium-ion (Li+) battery that powers the camera. In this article, we discuss the challenges of powering a digital camera and propose a new approach that saves power in addition to being more flexible.

Figure 1. DSLR Camera

DSLR Camera Block Diagram

Figure 2 shows the block diagram of a typical DSLR camera. The light is focused by the lens on the first mirror that, depending on its position, diverts the beam to the image sensor or to the viewfinder. The DDR memory stores the sensed images processed by the digital core and the sound collected from the built-in microphone.

DSLM cameras, by eliminating the mirrors and the viewfinder, places smaller lenses closer to the sensor, which reduces camera size and cost. Instead, an electronic viewfinder is utilized which has the disadvantage of a slight delay between the event shown and real time. Gyro stabilization is necessary for long range shoots, since the effects of camera shake are multiplied in long range images. Finally, the use of Wi-Fi allows wireless control of the camera allowing users to send photos straight to a smartphone for easy sharing on-the-go. All the electronics in these functional blocks are orchestrated by the main CPU and powered by a two-cell or a three-cell Li+ camera battery.

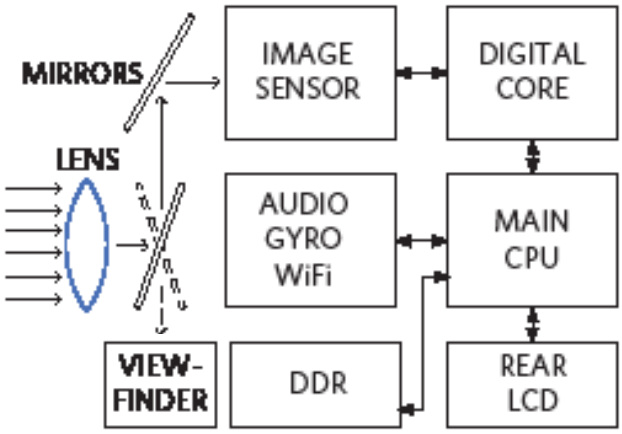

Figure 2. DSLR Camera Block Diagram

DSLR Camera Power (PMIC)

Figure 3 shows a generic PMIC buck that powers all the voltage rails and shows the current consumed by each block in operation, adding up to 6A.

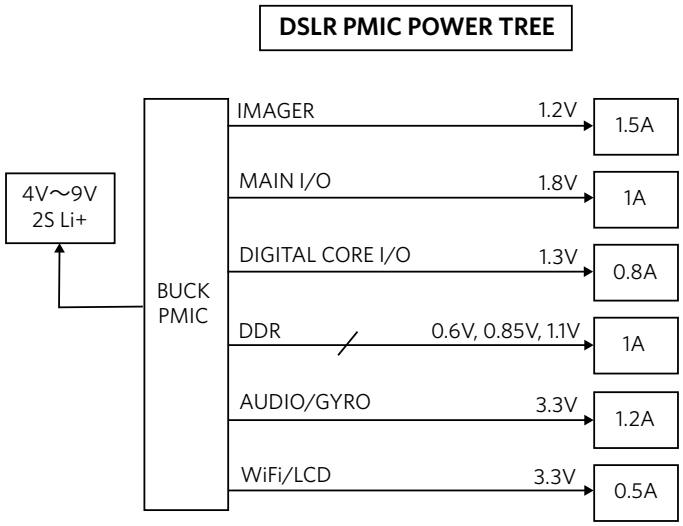

Figure 3. DSLR Camera Power Tree (PMIC)

A typical power source for DSLR cameras is a two-cell Li+ battery that delivers 7.2V and 1200mAh. Assuming for simplicity 90% efficiency and an average 2V output voltage utilized by buck regulators, the total input peak current is 6A x 2V/ (0.9 x 7.2V) = 1.85A. If this current were drawn continuously, it would discharge the battery in just 39 minutes (1200mAh/1.85A). This shows how important it is to save power in a digital camera.

The use of a PMIC requires a central location to minimize routing from the power supply to the load. With this approach, each power source is often far from the load. The floor planning of the PCB becomes critical and must avoid significant losses on the PCB traces.

As an example, if a 1.2V load draws 1.5A (1.8W) and has a distance of 20 squares of ½ ounce copper PCB trace from the PMIC (at 1mΩ/square), the trace will incur a power loss of 20 x 1m x 1.5^2 = 45mW. This corresponds to an efficiency loss of 2.5%, which is equivalent to taking your efficiency curve and lowering it down by two-and-a-half points. The camera run-time is shortened accordingly, robbing the camera user of those last few precious shots.

DSLR Camera Power (POL)

A better approach to powering the DSLR camera is through point-of-load (POL) architecture, as illustrated in Figure 4. In this case, a standalone regulator is placed close to the load it powers, eliminating the PCB routing issues and the power losses discussed earlier. Another advantage of the POL approach is scalability. A number of small buck regulators can be added or subtracted depending on the compexity of the power tree associated with a particluar DSLR camera model.

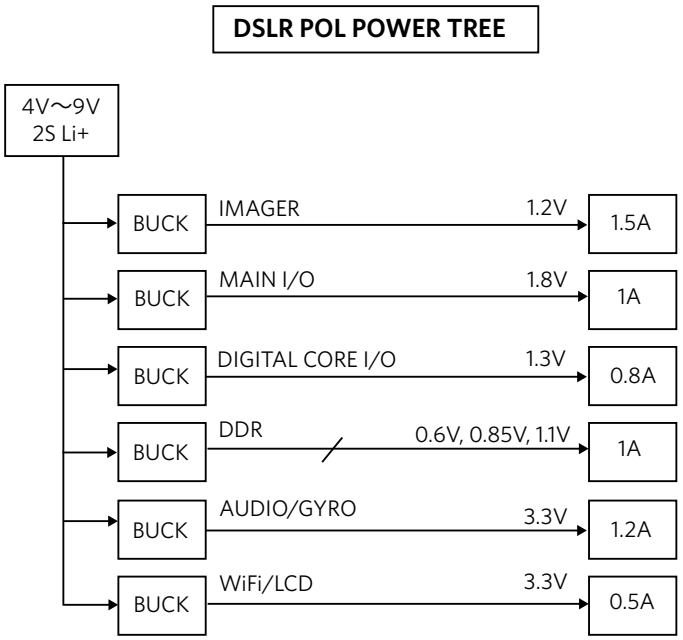

Figure 4. DSLR Camera Power Tree (POL)

POL Example

As an example, the MAX77503 is a synchronous 1.5A step-down DC-DC converter optimized for portable two-cell or three-cell, battery-operated or USB-C applications. This step-down converter can be used to individually power each of the required loads in the POL power tree of Figure 4. Thanks to the distributed POL architecture, the trace losses are avoided, with an efficiency gain in the order of 2.5% compared to the centralized PMIC approach shown in the previous section.

The converter operates on a 3V to 14V input supply. The output voltage is either adjustable between 0.8V and 5V in 50mV steps through an I^2C serial interface or 1.55V to 99% of the supply voltage with external feedback resistors. Factory-programmed default voltages of 1.2V, 1.8V, and 3.3V are offered to reduce component count for common rails by eliminating the external resistor-divider that sets the output voltage. Thanks to the integration of low $R_{DS(ON)}$ synchronous MOSFET transistors, the IC exhibits high efficiency at high load. The device also features a low-I_Q SKIP mode which allows excellent efficiency at light loads (Figure 5).

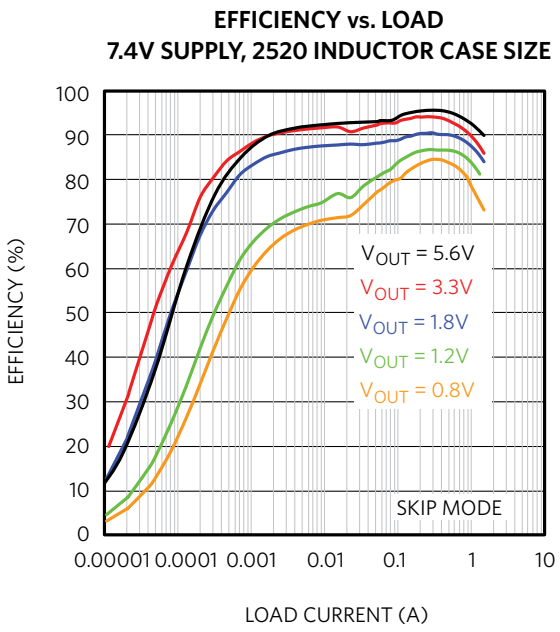

Figure 5. POL Buck Regulator Efficiency

The buck regulator is available in a 12-bump, 0.4mm pitch wafer-level package (WLP). Figure 6 shows the buck regulator's PCB size of 17.5mm^2 for a performance-optimized case (2520 inductor case), internal feedback version with pullups not drawn. A size-optimized PCB, with a 2016 inductor, uses only 14.3mm^2.

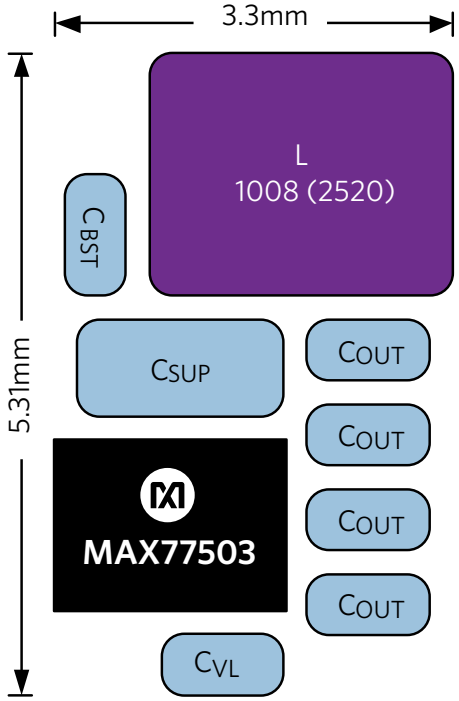

Figure 6. POL in a Performance-Optimized PCB (17.5mm^2)

The small-size occupancy of each POL helps minimize the size disadvantage of the distributed architecture, which utilizes multiple packages versus the PMIC which uses a single-package approach.

Conclusion

The high performance of DSLR/M cameras comes at a cost in terms of energy drawn from the Li+ battery. We showed that a POL system approach to power distribution within the digital camera saves power by minimizing the PCB traces losses. Scalability is another POL advantage, as a number of small buck regulators can be added or subtracted as needed, depending on the compexity of the digital camera. Accordingly, we proposed a high-efficiency, compact buck converter as the basic building block for the digital camera POL architecture.

Glossary

DSLR: Digital single lens reflex camera

DSLM: Digital single lens mirrorless camera (a.k.a. MILC)

ISO: International Standards Organization. A scale for measuring sensitivity to light.

MILC: Mirrorless interchangeable-lens camera

Learn more:

MAX77503 14V Input, 1.5A High-Efficiency Buck Converter with 9µA I_Q

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