DOCUMENT TITLE:

Product Reliability Qualification

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MOST RECENT CHANGES

FROM	TO
Revision I	Refer to next page for changes.

Add appendix 12.7	12.7 Wafer Level Chip Scale Package (WLCSP) reliability qualification requirements
5.4. New Section	5.4. AEC-Q100 – Automotive Electronics Council, Stress Test Qualification for Integrated Circuits
7.4.1.2. Appendix 12.3 lists discrete device level qualification tests. *Remove*	7.4.1.2. It is not necessary that all tests in Appendix 12.1, 12.2 and 12.3 must be performed for a product/process/package qualification. Only the relevant tests will be selected per the predefined qualification plan by the Rel group
7.4.1.3. It is not necessary that all tests in Appendix 12.1, 12.3 and 12.3 must be performed for a product/process/package qualification. Only the relevant tests will be selected per the predefined qualification plan by the Rel group.	7.4.1.3. Renumber to 7.4.1.2.
7.4.2.2. For discrete device level qualification, the sample sizes required are defined in Appendix 12.3. Any sample size reduction needs approval from Reliability management. *Remove* STRESS TEST NAME: Solder Reflow (convection reflow preferred) CONDITION: 85C/85% RH soak 168 hrs (or per MSL level) +245+/-5C peak 120-180 sec over 183 +SAM +Bond crater check	7.4.4.2. Automotive qualifications will use AEC-Q100 as a guideline for the development of the qualification plan. Any exceptions or additions to the requirements of this standard will be negotiated with the customer and/or clearly noted in the qualification plan.
7.4.5.2.1	**7.4.5.2.1 Added "…, or per J-STD-020D."**
7.4.5.2.2.	**7.4.5.2.2. Removed Infrared, changed reflow peak temperature to 240 +0°C/-5°C (Pb/Sn parts) or 260°C +0°C/-5°C (Pb-free parts) …**
7.5.5. New Section	7.5.5. For Wafer Level Chip Scale Package (WLCSP) product qualification, use Appendix 12.7 Wafer Level Chip Scale Package Reliability Qualification Requirements
12.1. RELIABILITY QUALIFICATION METHODS FOR IC'S IN PLASTIC PACKAGES STRESS TEST NAME: Temperature Cycle CONDITION: 65°C to 150°C 1000 X (note 1) Extended to 2000 X For information only. (note 1)	**12.1. RELIABILITY QUALIFICATION METHODS FOR IC'S IN PLASTIC PACKAGES** STRESS TEST NAME: Temperature Cycle (Note 6) CONDITION: Condition C 500x (-65°C to 150°C) or Condition B 1000x (- 55°C to 125°C) (note 1) *Add:* STRESS TEST NAME: Solder Reflow (convection reflow preferred) CONDITION: 85C/85% RH soak 168 hrs (or per MSL level) +240 +0/-5 peak reflow (lead/tin) or 260 +0/-5 peak reflow (lead-free) + SAM (optional) +Bond Crater NOTES: 6. For PCB-based Package in BGA, LGA, flipchip technology in molded packages, use only Temp Cycle condition B, 1000X in qualification. For CSP products, Temp cycling conditions is Slow Ramp (-40 C to +125 C, 1000X Ramp rate <15 C/min Dwell 15 minutes) with the same sampling and fail/pass criteria as regular one. 12.1 Added "(note 1)" to high temperature storage 12.1. Removed "IR" from Bond Crater Check condition 12.1. Changed plating thickness to 400u
12.2. RELIABILITY QUALIFICATION METHODS FOR IC'S IN HERMETIC PACKAGES STRESS TEST NAME: Temperature Cycle CONDITION: -65°C to +150°C/1000X extend to 2000 X for information only	**12.2. RELIABILITY QUALIFICATION METHODS FOR IC'S IN HERMETIC PACKAGES** STRESS TEST NAME: Temperature Cycle CONDITION: Condition C 500x (-65°C to 150°C) or Condition B 1000x (-55°C to 125°C) (note 1)
12.3. Discrete Device Level Reliability Qualification Guideline Table. *Table is revised. Added one paragraph.*	**12.3. Discrete Device Level Reliability Qualification Guideline** *Table is revised. Added the following paragraph.* Under the guideline of JEDEC standard JP-001, Foundry Process Qualification Guidelines, hot carrier injection (HCI) and Vt instability of MOS transistors, TDDB of gate oxide and MIM capacitor dielectrics, beta degradation of bipolar transistors and electro migration of metal connection system must be evaluated in order to project the device wear-out life time and to define the design rules and electric rules if such evaluation or similar evaluation has not been conducted before and the device is exposed to a significant reliability risk. It is REL's responsibility to assess the risk
12.4. RELIABILITY QUALIFICATION GUIDELINE FOR NEW PRODUCT/ FAB PROCES/ PACKAGE	

12.5. Guideline for qualification test matrix for major changes	Delete pressure pot test.
12.6.1. Long Term Reliability Monitor	Delete pressure pot test.
12.6.2.Short Term Reliability Monitor	Delete pressure pot test.
12.7, New Section	12.7 WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) RELIABILITY QUALIFICATION REQUIREMENTS.
8. Acceptance: Added 8.1.1. , statement for single random isolated failures.	8. Acceptance: 8.1.1. A single random isolated failure shall not constitute a qualification failure. In the event of a single failure, additional stress testing of a statistically sufficient sample size shall be conducted in order to demonstrate that the failure is not systematic to the process, package or product technology qualification, and the failure rate is within current reliability targets

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1. TITLE: Product Reliability Qualification

2. PURPOSE:

2.1. This specification establishes reliability qualification requirements for all Maxim IC devices.

3. SCOPE:

3.1. This specification applies to all IC devices manufactured by Maxim and Maxim's contractors. This includes all new products, fab processes, packages and major engineering changes on existing products.

4. TERMS AND DEFINITIONS:

4.1. It is the responsibility of the reliability group to carry out the qualification program with help from design, testing, packaging and production groups to make the qualification program successful.

5. APPLICABLE DOCUMENTS:

5.1. Mil-STD-883C - Test Methods and Procedures for Microelectronics

5.2. Mil-M-38510 - General Specification for Microcircuits

5.3. JEDEC Standard No.22A - Test Methods and Procedures for Solid State Devices used in Transportation/Automotive Applications

5.4. AEC-Q100 – Automotive Electronics Council, Stress Test Qualification for Integrated Circuits

6. EQUIPMENT AND MATERIALS:

6.1. As specified per test requirements.

7. GENERAL REQUIREMENTS:

7.1. QUALIFICATION PROGRAM REQUEST:

7.1.1. A written description by the submitting group of what is to be qualified shall be forwarded to Rel Department. The submission of qualification samples could be from Design, Process, Assembly/Packaging, or initiated by Reliability Group.

7.2. QUALIFICATION PLAN:

7.2.1. Upon receipt of the qualification request, Rel group shall publish a qualification plan that details:

7.2.1.1. Reliability testing required

7.2.1.2. Test condition and test duration

7.2.1.3. Sampling plan

7.2.1.4. Qualification schedule

7.2.1.5. Burn-in circuit and 85/85 test circuit if needed

7.3. QUALIFICATION SAMPLES:

7.3.1. It is the responsibility of submitting group to provide fully electrically tested (QA room) samples for product level qual and required test wafers for discrete device level qual to Rel group. This can be coordinated through the Product Line Managers (PLM).

7.3.2. For Major quals, 3 distinct lots are required. For Minor quals, 1 lot is required.

7.3.3. A control lot from existing qualified fab process or assembly process must be supplied along with the qualification samples, so that both groups may run in parallel through the qualification testing if necessary.

7.3.4. For discrete device level qual, number of lots required will be determined by Rel manager/director based on the significance level of the process change.

7.4. QUALIFICATION TEST:

7.4.1. Reliability Requirements:

7.4.1.1. Appendix 12.1 and 12.2. list standard qualification tests for plastic and hermetic packages. All plastic products shall be designed to survive the tests specified in Appendix 12.1. All hermetic products shall be designed to survive the tests specified in Appendix 12.2.

7.4.1.2. It is not necessary that all tests in Appendix 12.1, 12.2 and 12.3 must be performed for a product/process/package qualification. Only the relevant tests will be selected per the predefined qualification plan by the Rel group.

7.4.1.3. The exact qualification requirements will be governed by the qualification plan.

7.4.1.4. Qualification by similarity may be granted upon the discretion of the Reliability Management based upon past reliability information on closely similar packages, processes, or products.

7.4.1.5. Once qualified, a die type is considered qualified by extension to any other qualified package.

7.4.1.6. Once a core die type is fully qualified, only ESD and Latchup are required to extend qualification to die produced with other metal options.

7.4.2. Sampling Plan:

7.4.2.1 For product level qualification, the number of samples required is defined in Appendix 12.1 and 12.2. The accept/reject criteria are also listed in Appendix 12.1 and 12.2. The sample size of the tests may be adjusted if necessary per the LTPD sampling plan.

7.4.2.2 For high pin-count or high cost packages, sample sizes may be reduced.

7.4.3. Failure Definitions:

7.4.3.1. Devices which fail to meet endpoint inspection criteria shall be considered rejects. These endpoint inspections include electrical test, visual inspection, mechanical stress test, hermeticity test, destructive and non-destructive tests.

7.4.4. Special Customer Requirements:

7.4.4.1. In the event customer's requirements are more stringent than Appendix 12.1 and 12.2, the customer's requirements, as set forth in the special spec, shall be followed.

7.4.4.2. Automotive qualifications will use AEC-Q100 as a guideline for development of the qualification plan. Any exceptions or additions to the requirements of this standard will be negotiated with the customer and/or clearly noted in the qualification plan.

7.4.5. Pre-conditioning Requirements for Surface Mount Packages:

7.4.5.1. Plastic packages in surface mount forms should be subjected to preconditioning prior to the start of the following reliability tests: 85/ 85, HAST, and temperature cycling.

7.4.5.2. Surface Mount Packages should be subjected to:

7.4.5.2.1. 85 C/85 % R.H. environment with no bias for 168 hours; or per J-STD-020D.

7.4.5.2.2. Followed by 3 insertions through Reflow peak temperature 240 +0°C/-5°C (Pb/Sn parts) or 260°C +0°C/-5°C (Pb-free parts)

7.4.5.3. Electrical Test Verification:

7.4.5.3.1. Following the preconditioning test, all test samples should be electrically tested per data sheet specification.

7.4.6. Duration of Reliability Test:

7.4.6.1. For qualification purpose, each reliability test duration should follow the requirements specified in Appendix 12.1 and 12.2. Reliability stress testing should be extended to longer duration in order to determine process, package margin to the stated reliability performance.

7.4.6.2. Conditional qualification may be granted after passing 500 hours of burn-in, 500 hours of 85/85 (or HAST 100 hours). 168 hours of Pressure Pot, and 500 cycles of Temp. Cycle Test. before 1000 hours (or 1000 cycles) is completed. However, if the 1000 hour data fails the qual, customer shall be notified of qual results.

7.5. New Product/New Fab Process/New Package Qualification:

7.5.1. For the product level qualification of new fab process or new package or new assembly process, three manufacturing runs must satisfactorily meet the qualification requirements as defined in the qual plan. New products will be released for sampling or pre-production orders prior to the completion of the qualification plan. The qualification period will not extend longer than 90 days. The qualification results will then determine the status of continued production.

7.5.2. A new product, developed on an existing qualified process must complete successfully a life test monitor, prior to release for shipment. After three months, the product must demonstrate that its reliability performance meets Maxim's standard as outlined in Appendix 12.4 for new product qualification. If it does not, the product will be put on hold until an action plan is formulated and implemented to meet this goal. It is the responsibility of the Reliability Manager to govern and enforce this policy.

7.5.3. Qualifying product by similarity: The same die type does not need to be qualified in each available package/product configuration provided that (1) the die type has been successfully qualified in at least one package type, and (2) the same die type (process and function) has been qualified earlier in the intended package.

7.5.4. For a new fab process or a revised fab process, which justifies discrete device level qualification, a discrete device level qualification must be conducted. The data should be fed back to Fab to revise fab process and/or design rules if needed.

7.5.5. For Wafer Level Chip Scale Package (WLCSP) product qualification, use Appendix 12.7 Wafer Level Chip Scale Package Reliability Qualification Requirements. Three manufacturing runs (WLCSP) must be run for package (wafer) level reliability test and board level reliability test, to complete a full qualification.

7.6. Major Engineering Changes:

7.6.1. Major engineering changes are changes to the products that have the potential to adversely affecting product reliability. Examples of major engineering changes include the following:

7.6.1.1. Mask change or redesign

7.6.1.2. Metallization changes

7.6.1.3. Passivation or Dielectric changes

7.6.1.4. Major fab process changes

7.6.1.5. Packages changes

7.6.1.6. Molding compound changes

7.6.1.7. Wire bonding changes

7.6.1.8. Die attach changes

7.6.1.9. End of Line changes - deflash or plating method

7.6.2. All these changes may require product re-qualification and customer change notification per PCN procedure 10-0022..

7.6.3. Appendix 12.5 lists a guideline for qualification test matrix for major changes.

7.7. Burn-in Requirements:

7.7.1. Burn-in Evaluation for Qualification:

7.7.1.1. For each qualification test that requires a life test, a burn-in evaluation must be included to analyze the infant mortality of the process/product.

7.8. Failure Analysis of Qualification Failures

7.8.1. It is the responsibility of FA Engineering to analyze qualification rejects and issue an IFAR report in a timely manner so the cause of reject can be corrected.

7.9. Reliability Qualification Report

7.9.1. At the conclusion of the qualification effort, Rel engineering shall issue a reliability report to the appropriate groups.

7.9.2. All qualification reports will be submitted in electronic format for routing and approval. Approval shall include the originator, appropriate Rel Manager/Director, and the Executive Director of QA.

7.9.3. Approved electronic reports will be converted to PDF format and filed as defined by Reliability department .

7.10. Product Reliability Monitor Program

7.10.1. Once a product is qualified, the product will be in the monitor program. The product monitor lot selection shall be grouped by fab/process combination determined by QA and product groups.

7.10.2. Once per week, 80 units from a product representative of each major semiconductor process (i.e. S3, S5, etc.) shall have a life test (135°C/192 hours) and Pressure Pot 168 hours performed as a weekly monitor.

7.10.3. Once a quarter, a 1000 hours life test , a 1000 hours storage life test, a 1000 hours 85/85 test, and a 1000 cycles temperature cycle test, per Appendix 12.6, shall be performed to monitor each fab/process group.

7.10.4. The reliability monitor programs will be performed dependent upon availability of samples. In a monitor period where suitable samples are unavailable, the monitor interval will be skipped.

8. ACCEPTANCE:

8.1.1. A single random isolated failure shall not constitute a qualification failure. In the event of a single failure, additional stress testing of a statistically sufficient sample size shall be conducted in order to demonstrate that the failure is not systematic to the process, package or product technology qualification, and the failure rate is within current reliability targets.

9. DISPOSITION OF MATERIAL: N/A

10. DATA RECORDING:

10.1. All qualification samples and records shall be retained by the Rel Group for 5 years.

11. MAINTENANCE: N/A

12. APPENDICES:

13.

13.1. RELIABILITY QUALIFICATION METHODS FOR IC'S IN PLASTIC PACKAGES

STRESS TEST NAME	CONDITION	SAMPLING PLAN SS / Acc or LTPD (also ref. to 8.1.1)		END POINTS
Life Test, Dynamic preferable	135°C/ 1000 hrs with virgin production units only extend to 2000 hrs for information only	77 / 0	3%	Electrical
85/85 Temperature & Humidity Bias (THB) (Note 3)	85°C/85% RH, 1000 hrs extend to 2000 hrs for information only (note 1)	77 / 0	3%	Electrical
Pressure Pot (Autoclave) (Note 7)	121°C / 15 psig 168 hrs	77 / 0	3%	Electrical
HAST (Note 3)	130°C / 85% RH 100 hrs	45 / 0	5%	Electrical
Temperature Cycle (Note 6)	Condition C 500x (-65°C to 150°C) or Condition B 1000x (- 55°C to 125°C) (note 1)	77 / 0	3%	Electrical
High Temperature Storage	150°C/ 1000 hrs extend to 2000 hrs for information only (Note 1)	77 / 0	3%	Electrical
ESD	Human body model 1.5K ohm 100pF cap 2000V or actual Voltage	5 / 0		Electrical
Latch-up	+ / -200 mA or actual rating, using 1.5X VCC or absolute max ratings.	5 / 0		Electrical: requires post Latchup ATE tests
Power Cycle (Note 2)	Power On and off to cycle Tj between ambient and 150°C. 10k cycles minimum.	45/0	5%	Electrical
Solder Shock (Note 4)	260°C / 10 sec solder dip	15 / 0	15%	Electrical
Resist to Soldering Heat	300°C / 10 seconds	15 / 0	15%	Electrical
Wire Bond Pull	20 samples minimum pull all wires 5 grams minimum	20/0		accept no bond crater or oxide crack

STRESS TEST NAME	CONDITION	SAMPLING PLAN SS / Acc or LTPD (also ref. to 8.1.1)		END POINTS
Bond Crater Check	bake 125 C/24 hrs +Reflow +bond crater check	150/0 20/0		Post IR QA hot & room test Bond Crater & Visual test accept no crater or oxide crack
Die Shear	per Mil spec 883 method 2019.5	5 / 0		Must be provided by Assembly group
Physical Dimensions	per drawing	15 / 0	15%	Visual
Lead Fatigue	>3 90 degree bends	15 / 0	15%	Visual
Tensile Strength	8 oz weight / 30 sec	15 / 0	15 %	Visual
Solderability (Note 5)	minimum 8 hrs steam aging	15 / 0	15%	Visual
Resistance to Solvents		15 / 0	15%	Visual
Adhesion of Lead Finish		15 / 0	15%	Visual
Salt Atmosphere		15 / 0	15%	Visual
External Visual		15 / 0	15%	Visual
Plating Thickness	200u - inch min- Solder dip 400 u- inch min- Solder plating	10 / 0		
Solder Reflow (convection reflow preferred)	85C/85% RH soak 168 hrs (or per MSL level) +240 +0/-5C peak reflow (lead/tin) or 260 +0/-5 C peak reflow (lead-free) +SAM (optional) +Bond Crater	 150/0 20/0 20/0		 electrical (ref. J-STD-020D) accept no bond crater or oxide crack

NOTES:

1. Preconditioning is required for these tests per section 7.4.5 requirements.
2. High power devices only.
3. Either HAST or 85/85 may be chosen. However the following two cases are exception: A. Substrate-based packages (e.g., BGA, LGA), B. Packages with non conductive die attach. For these two exceptions only 85/85 test can be chosen.
4. For QFN package solder shock test is not required.
5. For SMD package (leaded or leadless) solderability test follows JESD 22 B102-C test method by dipping component termination 20 to 45 degree relative to flux and solder surface.
6. For PCB-based Package in BGA, LGA, flip-chip technology in molded packages, use only Temp Cycle condition B, 1000X in qualification.
   For CSP products, Temp cycling condition is Slow Ramp (–40 C to +125 C, 1000X Ramp rate <15 C/min Dwell 15 minutes) with the same sampling and fail/pass criteria as regular one.
7. Pressure Pot (Autoclave) is not recommended as a qualification test: Unbiased HAST or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave..

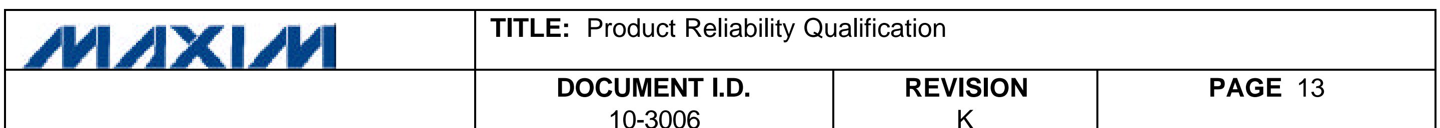
13.2. RELIABILITY QUALIFICATION METHODS FOR IC'S IN HERMETIC PACKAGES

STRESS TEST NAME	CONDITION	SAMPLING PLAN SS / Acc or LTPD (also ref. to 8.1.1)		END POINTS
Life Test, Dynamic	135°C/ 1000 hrs extend to 2000 hours for information only	77 / 0	3%	Electrical
Temperature Cycle	Condition C 500x (-65°C to 150°C) or Condition B 1000x (-55°C to 125°C) (note 1)	77 / 0	3%	Electrical + Seal
Thermal Shock	0°C to +100°C 200 cycles	77 / 0	3%	Electrical + Seal
High Temperature Storage	150°C/1000 hours Extend to 2000 hrs for information only	77 / 0	3%	Electrical
ESD	Human body model 2000V or actual Voltage	5 / 0		Electrical
Latch-up	+/-200 mA or actual rating, using 1.5x Vcc or absolute max ratings	5 / 0		Electrical
Solder Shock (Note1)	260°C/10 seconds solder dip	15 / 0	15%	Electrical + Seal
Resist to Soldering Heat	300°C/ 10 seconds	15 / 0	15%	Electrical
Wire Bond Pull	5 grams minimum	45 / 0	5%	
Die Shear	per Mil 883 method 2019.5	5 / 0		
Physical Dimensions	Per drawing	15 / 0	15%	Visual
Lead Fatigue	>3 90 degree bends	15 / 0	15%	Visual
Tensile Strength	8 oz weight/30 seconds	15 / 0	15%	Visual
Solderability (Note 2)	minimum 8 hours steam aging	15 / 0	15%	Visual

STRESS TEST NAME	CONDITION	SAMPLING PLAN SS / Acc or LTPD (also ref. to 8.1.1)		END POINTS
Resistance to Solvents		15 / 0	15%	Visual
Power Cycle	Power On and Off to cycle Tj between ambient and 150°C 10K cycles minimum	45 / 0	5%	Electrical
Salt Atmosphere		15 / 0	15%	Visual
RGA, Moisture Content	< 5000 PPM H_2O	3 / 0		
Mechanical Shock		15 / 0	15%	Electrical + Seal
Plating Thickness	200 u - inch min- Solder dip 300u- inch min Solder plating	10 / 0		
Lid Torque		5 / 0		Visual
Adhesion of Lead Finish		15 / 0	15%	Visual
External Visual		15 / 0	15%	Visual
Mil-Std-883, D-3 Thermal Sequence Thermal shock Temp cycle Moisture resistance Fine/Gross leak Visual Electrical	-55°C to +125°C, 15X -65°C to +150°C, 100X	45/0	5%	Seal + Visual + Electrical
Mil-Std-883, D-4 Mechanical Sequence Mechanical shock Vibration Const acceleration Fine/Gross leak Visual Electrical	Cond B Cond A Cond E	45 / 0	5%	Seal + Visual + Electrical

NOTES

1) For QFN package solder shock test is not required.
2) For SMD package (leaded or leadless) solderability test follows JESD 22 B102-C test method by dipping component termination 20 to 45 degree relative to flux and solder surface.



13.3. Discrete Device Level Reliability Qualification Guideline (Intrinsic Reliability)

Under the guideline of JEDEC standard JP-001, Foundry Process Qualification Guidelines, hot carrier injection (HCI) and Vt instability of MOS transistors, TDDB of gate oxide and MIM capacitor dielectrics, beta degradation of bipolar transistors and electromigration of metal connection system must be evaluated in order to project the device intrinsic life time and to define the design rules and electric rules if such evaluation or similar evaluation has not been conducted before and the device is exposed to a significant reliability risk. It is REL's responsibility to assess the risk level and to define the test methodology. The following table outlines the guideline for the evaluation:

TEST NAMES	STRESS CONDITIONS	SAMPLING PLAN	PASSING CRITERIA *	MAXIM SPEC
Hot Carrier Injection (NMOS)	• Vg at Max. Isub • Vds at acceleration voltatges with Vs=Vsub=GND • Room temperature. • Minimum channel length transistors for the specified applications.	3 DUTs per stress per device type.	1) For logic applications, ΔIdsat < 10% Idsat0. And ΔVt < 100mV 2) For analog applications, ΔGmmax < 10% Gmmax0, and ΔIdlin<10% Idlin0. Idsat is measured at Vds=Vgs=Vdd	Average life time = or > 100k hours at the specified maximum operational bias at room temperature. AC/DC ratio is determined based on the application of the device.
Vt Instability (NBTI) PMOS	• Vg at maximum operational voltage • Vs=Vd=Vsub=GND • 150°C, 168 hrs. • Minimum channel length transistors for the specified applications.	3 DUTs per stress per device type.	1) For logic applications, ΔVt abs value < 100mV 2) For analog applications, per IOS Vt is measured at room temperature. DUTs are cooled with bias stress on.	Zero DUT fails.
Gate Oxide TDDB	• Vg at acceleration voltages in accumulation mode. • NMOS and PMOS • 150°C	12 DUTs per stress voltage per device type.	< 10x leakage current increase.	Time to 0.1% (T0.1) fail at maximum operational voltage at 150C = or > 100k hours.
MIM cap TDDB	• V at acceleration voltages. • Intrinsic MIM cap • 150°C	12 DUTs per stress voltage per device.	< 10x leakage current increase.	Time to 0.1% (T0.1) fail at the maximum operational voltage at 150C = or > 100k hrs.
Electromigration	• Metal lines on worst topographic features. • Worst metal width, contact and via sizes.	12 DUTs per stress per device type	< 20% resistance increase.	Time to 0.1% (T0.1) fail at the specified maximum current density and temperatures = or > 100k hours.
Beta Degradation of Bipolar	• For E-B reverse stress, stress at room temperature.	3 DUTs per stress per device type.	< 10% beta drift.	Average life time at the specified maximum operational bias at room temperature = or > 100k hours.

- The passing criteria may be adjusted based on the requirement specified in process or product IOS of the specific product or process. The criteria listed in this table are the general guideline.

13.4. RELIABILITY QUALIFICATION GUIDELINE FOR NEW PRODUCT/ FAB PROCESS/ PACKAGE*4

TEST NAME	NEW PRODUCT		NEW FAB PROCESS		NEW PACKAGE/ ASSEMBLY PROCESS	
	TEST CONDITION	SAMPLING PLAN	TEST CONDITION	SAMPLING PLAN	TEST CONDITION	SAMPLING PLAN
Life Test	135°C/192 hrs*1	77 / 0 or 45/0	135°C/1000 hrs	77 / 0	135°C/1000 hrs	77 / 0
85 / 85 Test *1			1000 hrs	77 / 0	1000 hrs	77 / 0
Pressure Pot *1 *3			168 hrs	77 / 0	168 hrs	77 / 0
Temp Cycle Cond. B or Cond C			1000 X Cond B 500 X Cond C	77 / 0	1000 X Cond B 500 X Cond C	77 / 0
HAST *1 130°C/85% R.H.			100 hrs	45 / 0	100 hrs	45 / 0
ESD	YES					
Latch-up	YES					
Bondwire Pull			Yes	20/0	Yes	20/0
Bond Crater Check			Yes	20/0	Yes	20/0

*1 Plastic packages only

*2 Standard Burn In temperature is Ta = 135°C. Other temperatures and durations may be substituted for products with high power dissipation, or with component limitation to high temperature performance.

*3 Pressure Pot (Autoclave) is not recommended as a qualification test: Unbiased HAST or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave.

*4 Also ref. to 8.1.1

13.5. GUIDELINE FOR QUALIFICATION TEST MATRIX FOR MAJOR CHANGES

	New Fab Location	New Fab Process	Passivation	Metal	Dielectric	Starting Wafer	New Assembly	New Package	Plastic Molding Compound	Die Attach	Wire Bond	Die coating	Lead Finish
Life Test	X	X	X	X	X	X	X	X	X	X	X	X	
85/85	X	X	X	X	X		X	X	X	X		X	X
Temp. Cycle	X	X	X	X	X		X	X	X	X	X	X	
High Temp. Storage	X	X	X	X			X	X	X		X	X	
Hast *1	X	X	X	X	X		X	X	X	X		X	X
Power Cycle	X*2	X*2		X*2			X*2	X*2		X*2	X		
ESD	X	X				X							
Latch-Up	X	X				X							
Solder Reflow							X	X	X	X	X	X	
Solderability							X	X					X
Resist to Solvents							X	X	X				
Solder Shock							X	X	X	X	X	X	
Wire Bond Pull	X	X		X			X	X	X	X	X	X	
Bond Crater Check	X	X		X	X		X	X	X	X	X		
Shock, Vibration Centrifuge *3							X	X		X	X		

Note: X = Mandatory
*1 = Optional
*2 = Power devices only
*3 = Hermetic only

13.6. PRODUCT RELIABILITY MONITOR PROGRAM

13.6.1. LONG TERM RELIABILITY MONITOR

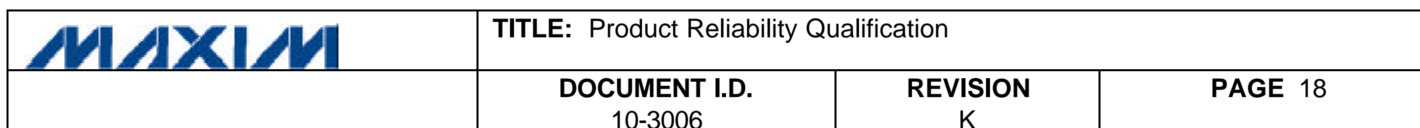
TEST	TEST CONDITIONS	SAMPLING PLAN SS/Acc (also ref. to 8.1.1)	FREQUENCY
Life Test	135°C/1000 hrs	77 /0	per quarter
85 / 85 Test	1000 hrs	77 / 0	per quarter
Temp Cycle	1000 cycles	77 / 0	per quarter
High Temp Storage Life	150°C/1000 hrs	77 / 0	per quarter

13.6.2. SHORT TERM RELIABILITY MONITOR

TEST	TEST CONDITIONS	SAMPLING PLAN SS/Acc (also ref. to 8.1.1)	FREQUENCY
Life Test	135°C/192 hrs	77/ 0	per week

12. 7 WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) RELIABILITY QUALIFICATION REQUIREMENTS

Parameter or Item	Specifications	Present Capability	Unit	Comments	Sampling Plan[1,2]	# of Lots
Package/Die Level Tests						
High Temp. Bake (Storage Life)	JESD22 A103	1,000	Hours	Storage at +150 °C w/o Bias	0/77	3
Solder Reflow MSL1	J-STD 20C	3	cycles	260°C peak temperature, MSL 1	0/150	3
Board Level Tests		To be Tested WITHOUT Underfill.		Test module with high Tg, FR4, 41mil substrate (40L PDIP 600mil) for board-level TC and THB. Drop Test per JESD22 B111 board definition.		
Operating Life Test (OP Life)	JESD22 A108	1,000	Hours	Tj=+135 °C	0/77	3
Drop Test (Daisy chain die mounted on PCB)	JESD22 B111	150	Pulses	1500 g's ± 10%, 0.5 ms half-sine wave	0/60 [3]	1
Temp. Cycle (TC) Slow Ramp	JESD22 A104, Condition G	1,000	Cycles	-40°C to +125°C, 15 minutes ramp (ramp rate 11 C/min), 15 minutes dwell, 1 cycle/hr	0/77	3
Temp Humidity Bias (THB) Test (Optional)	JESD22 A101	1,000	Hours	Ta=85 C, 85 % RH, biased	0/77	3
Temp. Cycle Sony Ericsson Fast Ramp (Optional)	Per Sony specification	500	Cycles	-25°C to +125°C, fast ramp, Dwell=10 minutes, 3 cycles/hr	0/77	3
Temp. Cycle Sony Ericsson Slow Ramp (Optional)	Per Sony specification	800	Cycles	-40°C to +100°C, 15 minutes ramp (ramp rate 11 C/min), 15 minutes dwell, 1 cycle/hr	0/77	3



Notes
1. For high pin-count or high cost packages, samples sizes may be reduced. (also see 7.4.2.2)
2. A single random isolated failure shall not constitute a qualification failure. In the event of a single failure, additional stress testing of a statistically sufficient sample size shall be conducted in order to demonstrate the failure is not systematic to the process, package or product technology qualification and the failure rate is within current reliability targets. (also see 8.1.1)
3. Total of 60 CSP die from 4 PCB, 15 daisy chain die per board. Generic drop test data from the highest ball array CSP die in a CSP technology is acceptable to support CSP qualifications for smaller ball array CSP die.

0	ECN 6988. Initial release.	04/06/90	PL
A	ECN B6892. To reflect policy/procedure changes.	06/15/92	KH
B	ECN C0665. To update current reliability test method and test conditions.	10/14/92	PL
C	ECN D4138. To update current reliability test method and requirements.	04/17/95	PL
D	ECN E5370. To update current reliability test requirements. Change **From:** 7.3.2. It is generally a good idea, though not a requirement, that samples from a control lot (existing qualified product) be supplied along with the qualification samples, so that samples from the two lots can be run in parallel through the qualification testing. 7.7.2 Production Burn-in: 7.7.2.1 All revenue units must be burned-in for at least 24 hours for new products. For mature products, this requirement may be adjusted to 12 hours if burn-in evaluation results justify. Flow 2 products are not subjected to this requirement. 12.1 Vapor Phase Reflow Or Infrared Solder Reflow 220°C/90 seconds in vapor phase zone Total 3 times 220°C/ 90 seconds Total 3 times 45/ 0 45 / 0 Electrical 12.1 Continued: Wire Bond Pull On line 5 grams minimum 45 / 0 5% **TO:** 7.3.2 A control lot from existing qualified fab process or assembly process must be supplied along with the qualification samples, so that samples from two lots can be run in parallel through the qualification testing. 7.7.2 Delete section. 7.7.2.1 Delete section. 12.1 Vapor Phase Reflow Or Infrared Solder Reflow 5C/85% RH soak 168 hrs+VPR & Infrared 220C/90 sec/3X +SAM +Bond crater check 0/150 0/20 0/20 hot & room test accept no bond crater or oxide crack Add note: If a moisture soak or bake is specified prior to VPR or IR reflow, change the condition accordingly. 12.1 Continued: Wire Bond Pull 20 samples minimum pull all wires 5 grams minimum 0/20 accept no bond crater or oxide crack Add to 12.1 under Wire Bond Pull: Bond Crater Check bake 125 C/24 hrs +VPR +bond crater check 0/150 0/20 hot & room test accept no crater or oxide crack	10-11-96	PL
E	ECN E5982: Add section 8.4: This reliability monitor program will be done based on the availability of samples. In the monitor period where no sample is available, this monitor program will be skipped.	1/13/97	PL
F	ECN MFN-99-7048. Canceled Per Bryan Preeshl	6/9/99	DM
G	ECN HQ-99-1212. Update reliability monitor program. Eliminate preconditioning for pressure pot. Require post Latchup ATE tests. Revise ESD acceptance language. Add "qualification by similarity" declaration language. Burnin not required unless by cust. spec. Specify virgin units only for long term BI eval. Conditional qualification is allowed with 3 lots of acceptable BI data at least 500 hour/lot. Pressure Pot qualification now lists LTPD for acceptance. List Hast test sampling plan as 5% LTPD. Control samples are recommended but not required to be run along with Qual experimental samples.	9/27/99	MH
H	ECN HQ-01-2264. To include new requirements for approval and filing of Maxim Qualification Reports.	6/27/01	BP
I	ECN HQ-02-5221. Add discrete device reliability test methodology and specification.	6/16/04	CC/PL
J	CANCELED	09-26-07	CC/PL
K	ECN EV-07-1510. Add discrete device reliability test methodology and specification. Add AEC-Q100 requirement. Revise TCT condition. Add WLCSP qualification requirements. Add 8.1.1. Acceptance conditions.	10-05-07	CC/PL/TT

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