

RELIABILITY REPORT
FOR
MAX9281GTM+T
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

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Conclusion

The MAX9281GTM+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9277/MAX9281 are 3.12Gbps Gigabit Multimedia Serial Link (GMSL) serializers with 3- or 4-data lane LVDS input (oLDI) and a CML serial output programmable for 50 coax or 100 shielded twisted pair (STP) cable drive. The MAX9281 has HDCP content protection but otherwise is the same as the MAX9277. The serializers pair with any GMSL deserializer capable of coax input. When programmed for STP output they are backward compatible with any GMSL deserializer. The output amplitude is programmable 100mV to 500mV single-ended (coax) or 100mV to 400mV differential (STP). The audio channel supports L-PCM I2S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits. The embedded control channel operates at 9.6kbps to 1Mbps in UART-UART and UART-I2C modes, and up to 1Mbps in I2C-I2C mode. Using the control channel, a μ C can program serializer, deserializer and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9281). A GPO output supports touch-screen controller interrupt requests from the remote end of the link. For use with longer cables, the serializers have programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC61000-4-2 ESD standards. The core supply is 1.7 to 1.9V and the I/O supply is 1.7 to 3.6V. The package is a lead-free, 48-pin, 7mm x 7mm TQFN with exposed pad and 0.5mm lead pitch.

II. Manufacturing Information

A. Description/Function:	3.12Gbps GMSL Serializers for Coax or STP Output Drive and LVDS Input
B. Process:	TS18
C. Number of Device Transistors:	724722
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	August 30, 2013

III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5109
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	165.3543 X 166.9291 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.9 \times 10^{-9}$$

$$\lambda = 13.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.1 @ 25°C and 1.9 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QANQ1A004B, D/C 1325)

The HS57-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9281GTM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	QANQ0A004A, D/C 1325

Note 1: Life Test Data may represent plastic DIP qualification lots.