

RELIABILITY REPORT
FOR
MAX6713REXS
PLASTIC ENCAPSULATED DEVICES

October 15, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX6713 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6713 is a microprocessor (μP) supervisory circuit used to monitor the power supplies in μP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5.0V, +3.3V, +3.0V, or +2.5V-powered circuits. It also provide a debounced manual reset input.

This circuit asserts a reset signal whenever the V_{CC} supply voltage declines below a preset threshold or whenever manual reset is asserted. Reset remains asserted for at least 140ms after V_{CC} has risen above the reset threshold or when manual reset is deasserted. Reset thresholds suitable for operation with a variety of supply voltages are available.

The MAX6713 has an open-drain output stage. The MAX6713's open-drain RESET-bar output requires a pull-up resistor that can be connected to a voltage higher than V_{CC} . The MAX6713 has an active-low reset output. The reset comparator is designed to ignore fast transients on V_{CC} , and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1V.

Low supply current makes the MAX6713 ideal for use in portable equipment. This device is available in a 4-pin SC70 package.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|---|--|
| Terminal Voltage (with respect to GND) | |
| VCC | -0.3V to +6.0V |
| RESET, RESET (push-pull) | -0.3V to ($V_{\text{CC}} + 0.3\text{V}$) |
| RESET (open drain) | -0.3V to +6.0V |
| MR | -0.3V to ($V_{\text{CC}} + 0.3\text{V}$) |
| Input Current, VCC, MR | 20mA |
| Output Current, RESET, RESET | 20mA |
| Rate of Rise, VCC | 100V/ μs |
| Operating Temperature Range | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation ($T_{\text{A}} = +70^\circ\text{C}$) | |
| 4-Pin SC70 | 245mW |
| Derates above +70°C | |
| 4-Pin SC70 | 3.1mW/ $^\circ\text{C}$ |

II. Manufacturing Information

| | |
|----------------------------------|--|
| A. Description/Function: | 4-Pin SC70 Microprocessor Reset Circuits with Manual Reset Input |
| B. Process: | S8 - Standard 8 micron silicon gate CMOS |
| C. Number of Device Transistors: | 380 |
| D. Fabrication Location: | California, USA |
| E. Assembly Location: | Malaysia |
| F. Date of Initial Production: | March, 2000 |

III. Packaging Information

| | |
|---|---------------------------|
| A. Package Type: | 8-Lead NSO |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Alloy 42 |
| D. Die Attach: | Non-Conductive Epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | Buildsheet # 05-1601-0100 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 30 X 30 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | TiW/ AlCu/ TiWN |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | .8 microns (as drawn) |
| F. Minimum Metal Spacing: | .8 microns (as drawn) |
| G. Bondpad Dimensions: | 2.7 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.79 \times 10^{-9} \quad \lambda = 6.79 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5033) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at <http://www.maxim-ic.com>.

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS42-4 die type has been found to have all pins able to withstand a transient pulse of $\pm 600\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 200\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX6617REXS

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|--------------------|---------------------------|
| Static Life Test (Note 1) | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | 160 | 0 |
| Moisture Testing (Note 2) | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} 3/ | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.

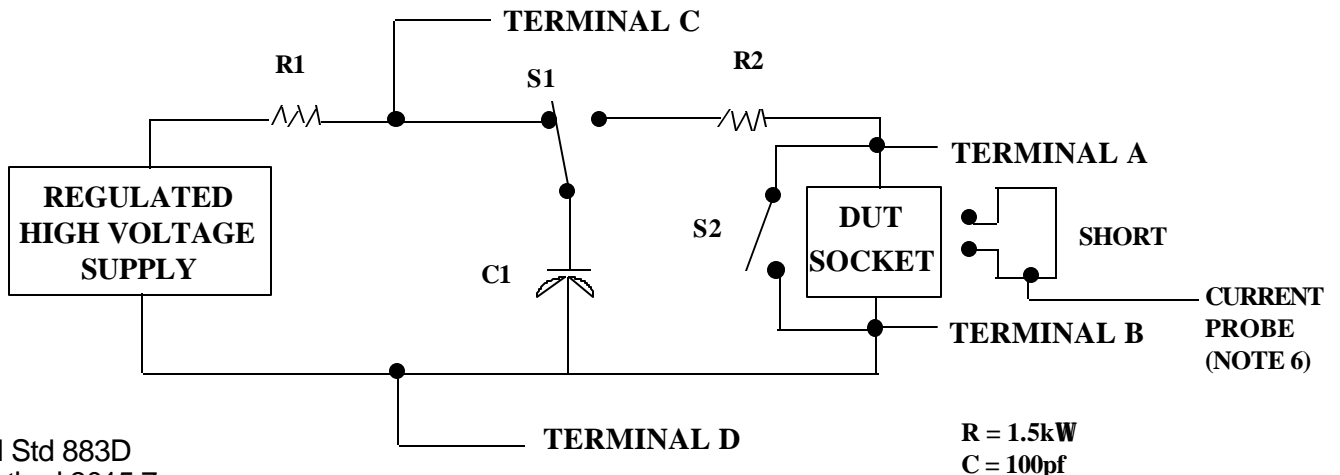
2/ No connects are not to be tested.

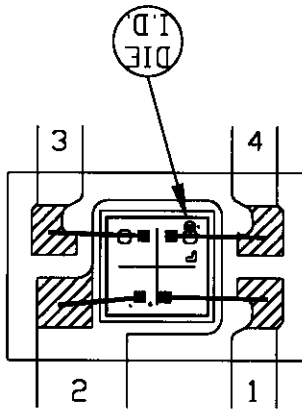
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.






USE NON-CONDUCTIVE EPOXY

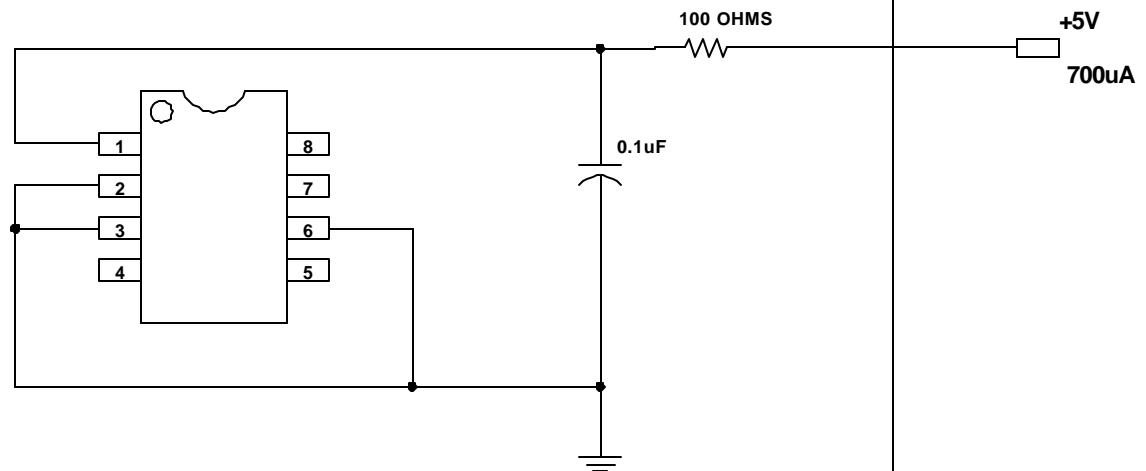
 BONDABLE AREA

NOTE: CAVITY DOWN

| | | | | | |
|----------------------|-------------|-----------|------|---|--------|
| PKG.CODE: X4-1 | | APPROVALS | DATE |  | |
| CAV./PAD SIZE: 34x35 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1601-0100 | REV: A |

ONCE PER SOCKET

ONCE PER BOARD



8-DIP

DEVICES: MAX 941/809/810/823/824/825/803
MAX 6381/6835
MAX. EXPECTED CURRENT = 700uA AND 15uA

DRAWN BY: HAK TAN
NOTES: 15 uA FOR MAX 6381