RELIABILITY REPORT

FOR

MAX668EUB

PLASTIC ENCAPSULATED DEVICES

June 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by  Reviewed by

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Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX668 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX668 constant-frequency, pulse-width-modulating (PWM), current-mode DC-DC controller is designed for a wide range of DC-DC conversion applications including step-up, SEPIC, flyback, and isolated output configurations. Power levels of 20W or more can be controlled with conversion efficiencies of over 90%. The 1.8V to 28V input voltage range supports a wide range of battery and AC-powered inputs. An advanced BiCMOS design features low operating current (220 $\mu$A), adjustable operating frequency (100kHz to 500kHz), soft-start, and a SYNC input allowing the MAX668 oscillator to be locked to an external clock.

DC-DC conversion efficiency is optimized with a low 100mV current-sense voltage as well as with Maxim’s proprietary Idle Mode™ control scheme. The controller operates in PWM mode at medium and heavy loads for lowest noise and optimum efficiency, then pulses only as needed (with reduced inductor current) to reduce operating current and maximize efficiency under light loads. A logic-level shutdown input is also included, reducing supply current to 3.5$\mu$A.

The MAX668 operates with inputs as low as 3V and can be connected in either a bootstrapped or non-bootstrapped (IC powered from input supply or other source) configuration. When not bootstrapped, it has no restriction on output voltage. The MAX668 IC is available in an extremely compact 10-pin $\mu$MAX package.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ to GND</td>
<td>-0.3V to +30V</td>
</tr>
<tr>
<td>PGND to GND</td>
<td>±0.3V</td>
</tr>
<tr>
<td>SYNC/SHDN to GND</td>
<td>-0.3V to +30V</td>
</tr>
<tr>
<td>EXT, REF to GND</td>
<td>-0.3V to $(V_{LDO} + 0.3V)$</td>
</tr>
<tr>
<td>LDO, FREQ, FB, CS+ to GND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>LDO Output Current</td>
<td>-1mA to +20mA</td>
</tr>
<tr>
<td>REF Output Current</td>
<td>-1mA to +1mA</td>
</tr>
<tr>
<td>LDO Short Circuit to GND</td>
<td>Momentary</td>
</tr>
<tr>
<td>REF Short Circuit to GND</td>
<td>Continuous</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation</td>
<td></td>
</tr>
<tr>
<td>(TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>10-Pin $\mu$MAX</td>
<td>444mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>10-Pin $\mu$MAX</td>
<td>5.6W/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: 1.8V to 28V Input, PWM Step-Up Controllers in µMAX

B. Process: S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS

C. Number of Device Transistors: 1861

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Malaysia, Thailand or Philippines

F. Date of Initial Production: July, 1998

III. Packaging Information

A. Package Type: 10-Lead µMAX

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1101-0021

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 58 X 80 mils

B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: iO$_2$

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:  
   Jim Pedicord (Manager, Rel Operations)  
   Bryan Preeshl (Executive Director)  
   Kenneth Huening (Vice President)  

B. Outgoing Inspection Level:  
   0.1% for all electrical parameters guaranteed by the Datasheet.  
   0.1% For all Visual Defects.  

C. Observed Outgoing Defect Rate:  < 50 ppm  

D. Sampling Plan:  Mil-Std-105D  

VI. Reliability Evaluation

A. Accelerated Life Test  

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:  

   \[
   \lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2} 
   \]  
   (Chi square value for MTTF upper limit)  

   Temperature Acceleration factor assuming an activation energy of 0.8eV  

   \[
   \lambda = 13.57 \times 10^{-9} 
   \]  

   \[
   \lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)} 
   \]  

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5266) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).  

B. Moisture Resistance Tests  

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.  

C. E.S.D. and Latch-Up Testing  

   The PX02 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
### Table 1
Reliability Evaluation Test Results

**MAX668EUB**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C</td>
<td>DC Parameters &amp; functionality</td>
<td>80</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Biased</td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Pressure Pot</td>
<td>DC Parameters &amp; functionality</td>
<td>uMAX</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Ta = 121°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P = 15 psi.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time = 168 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85/85</td>
<td>Ta = 85°C</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Temperature</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Cycle</td>
<td>-65°C/150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Method 1010</td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Each pin individually connected to terminal A</td>
<td>(The common combination of all like-named pins</td>
</tr>
<tr>
<td></td>
<td>with the other floating)</td>
<td>connected to terminal B)</td>
</tr>
<tr>
<td>1.</td>
<td>All pins except V_{PS1} 3/</td>
<td>All V_{PS1} pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
   (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_{S}, -V_{S}, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8