RELIABILITY REPORT

FOR

MAX16914AUB+

PLASTIC ENCAPSULATED DEVICES

November 21, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX16914AUB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX16914/MAX16915 low-quiescent-current overvoltage and reverse-battery protection controllers are designed for automotive and industrial systems that must tolerate high-voltage transient and fault conditions. These conditions include load dumps, voltage dips, and reversed input voltages. The controllers monitor the input voltage on the supply line and control two external pFETs to isolate the load from the fault condition. The external pFETs are turned on when the input supply exceeds 4.5V and stay on up to the programmed overvoltage threshold. During high-voltage fault conditions, the controllers regulate the output voltage to the set upper threshold voltage (MAX16915), or switch to high resistance (MAX16914) for the duration of the overvoltage transient to prevent damage to the downstream circuitry. The overvoltage event is indicated through an active-low, open-drain output, active-low OV. The reverse-battery pFET behaves as an ideal diode, minimizing the voltage drop when forward biased. Under reverse bias conditions, the pFET is turned off, preventing a downstream tank capacitor from being discharged into the source. Shutdown control turns off the IC completely, disconnecting the input from the output and disconnecting TERM from its external resistor-divider to reduce the quiescent current to a minimum. Both devices are available in a 10-pin µMAX® package, and operate over the automotive -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	Ideal Diode, Reverse-Battery, and Overvoltage Protection Switch/Limiter Controllers with External MOSFETs
B. Process:	S45
C. Number of Device Transistors:	2257
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Philippines or Thailand
F. Date of Initial Production:	October 23, 2009

III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3774
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	54X54 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.4 \times 10^{-9}$

λ = 11.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.04 @ 25C and 0.69 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SPGYCQ001C, D/C 0927)

The NR05-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX16914AUB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	SPGYCQ001C, D/C 0927
	Biased	& functionality	48	0	SPGZCQ001C, D/C 0927
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.