RELIABILITY REPORT

FOR

MAX1518BETJ

PLASTIC ENCAPSULATED DEVICES

July 5, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX1518 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1518B includea a high-performance step-up regulator, two linear-regulator controllers, and high-current operational amplifiers for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs). Also included is a logic-controlled, high-voltage switch with adjustable delay.

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The converter is a high-frequency (1.2MHz) current-mode regulator with an integrated 14V n-channel MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while achieving efficiencies over 85%.

The gate-on and gate-off linear-regulator controllers provide regulated TFT gate-on and gate-off supplies using external charge pumps attached to the switching node. The MAX1518 includes five high-performance operational amplifiers. This amplifier is designed to drive the LCD backplane (VCOM) and/or the gamma-correction divider string. The device features high output current (±150mA), fast slew rate (13V/µs), wide bandwidth (12MHz), and rail-to-rail inputs and outputs.

The MAX1518B is available in 32- pin thin QFN packages with a maximum thickness of 0.8mm for ultra-thin LCD panels.

B. Absolute Maximum Ratings

Item	Rating
IN, CTL to AGND	-0.3V to +7V
COMP, FB, FBP, FBN, DEL, REF to AGND	-0.3V to (VIN + 0.3V)
PGND, BGND to AGND	±0.3V
LX to PGND	-0.3V to +14V
SUP to AGND	-0.3V to +14V
DRVP, SRC to AGND	-0.3V to +30V
POS_, NEG_, OUT_ to GND	-0.3V to (VSUP + 0.3V)
DRVN to AGND	(VIN - 30V) to (VIN + 0.3V)
COM, DRN to AGND	-0.3V to (VSRC + 0.3V)
DRN to COM	-30V to +30V
OUT_ Maximum Continuous Output Current	±75mA
LX Switch Maximum Continuous RMS Output Current	1.6A
Continuous Power Dissipation (TA = +70°C)	
32-Pin Thin QFN (derate 21.2mW/°C above +70°C)	1702mW
Operating Temperature Range	-40°C to +100°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	TFT-LCD DC-DC Converters with Operational Amplifiers
B. Process:	B8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	4608
D. Fabrication Location:	Texas or California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	April, 2004

III. Packaging Information

A. Package Type:	**32-Lead QFN (5x5)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0618
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	122 X 137 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 41 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 26.82 \times 10^{-9}$ λ = 26.82 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6177) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**) located on the Maxim website at http://www.maxim-ic.com . Current monitor data for the B8/S8 Process results in a FIT rate of 0.27 @ 25°C and 4.64 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PD35-5 die type has been found to have all pins able to withstand a transient pulse of <±500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current ofv±250mA.

Table 1
Reliability Evaluation Test Results

MAX1518BETJ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	41	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

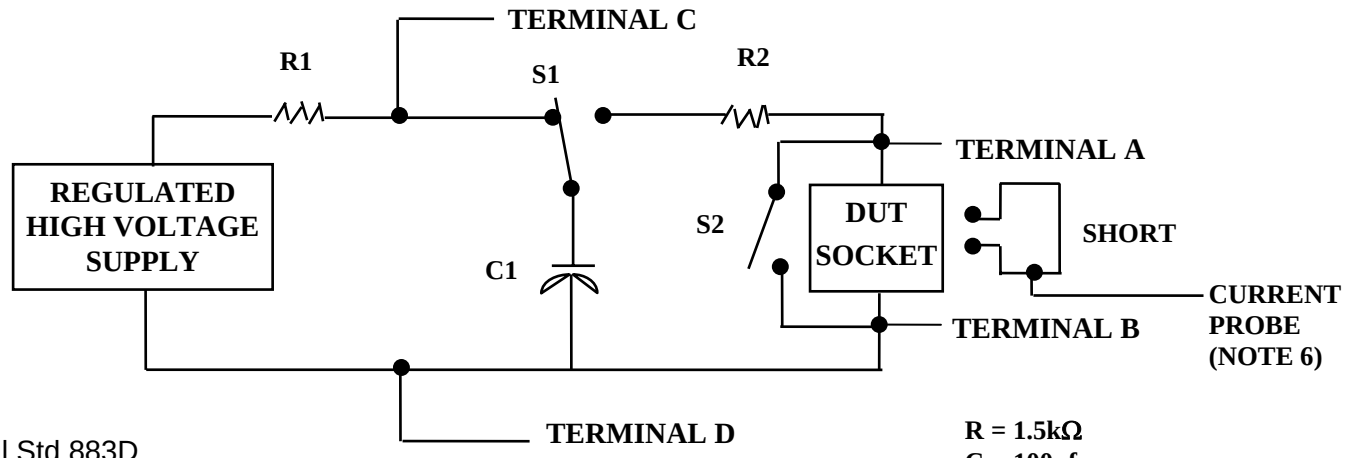
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

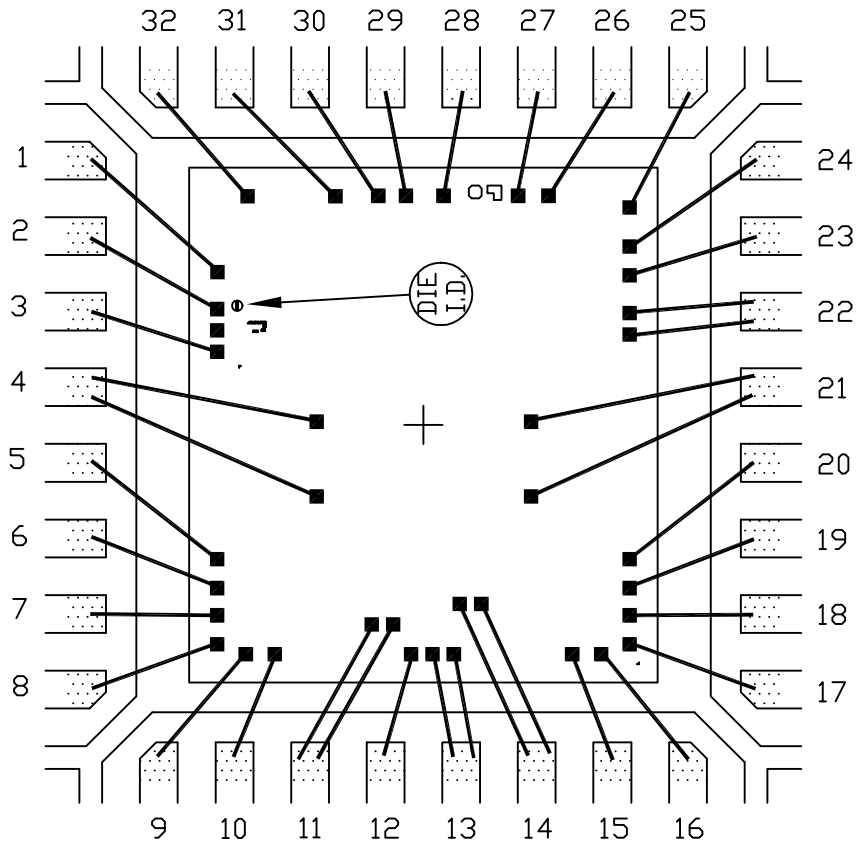
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



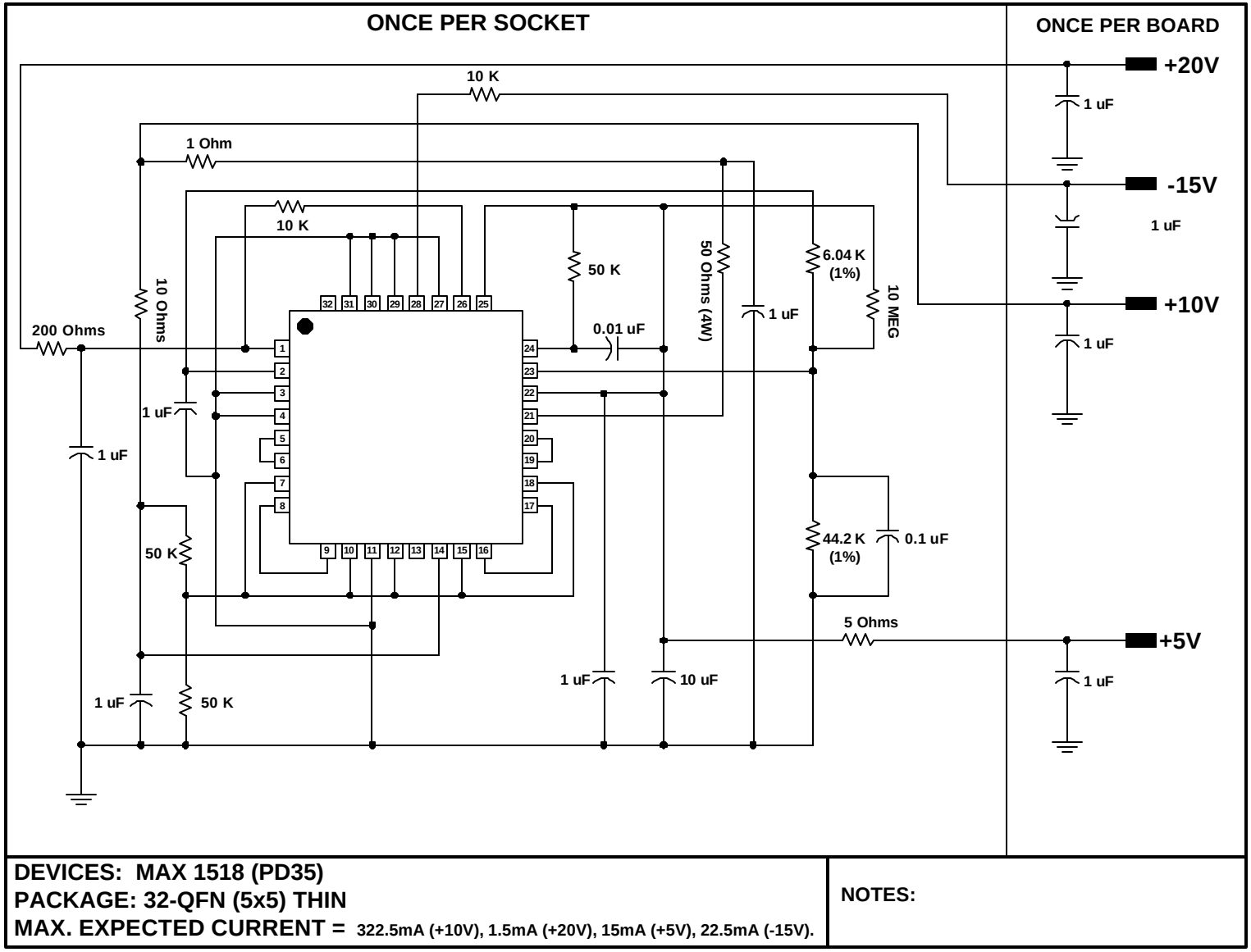
Mil Std 883D
Method 3015.7
Notice 8

5x5x0.8mm THIN QFN PKG. EXPOSED PAD PKG.



BONDABLE AREA

PKG. CODE: T3255-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 150x150	PKG.			BOND DIAGRAM #: 05-9000-0618	REV: C
	DESIGN				



DEVICES: MAX 1518 (PD35)
PACKAGE: 32-QFN (5x5) THIN
MAX. EXPECTED CURRENT = 322.5mA (+10V), 1.5mA (+20V), 15mA (+5V), 22.5mA (-15V).

NOTES: