RELIABILITY REPORT

FOR

MAX14895EETE+

PLASTIC ENCAPSULATED DEVICES

June 10, 2015

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| Approved by |
| --- |
| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

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**Conclusion**

The MAX14895EETE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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## I. Device Description

A. General

The MAX14895E integrates level-translating buffers and features RED, GRN, and BLU (RGB) port protection for VGA signals. The device has horizontal sync (SYNCH_) and vertical synch (SYNCV_) translating buffers that convert low-level CMOS inputs from a graphics controller to meet full 5V, TTL-compatible outputs. Each output can drive ±10mA and meets the VESASM specification. In addition, the device translates the direct digital control (DDC) signals to a lower level that is safe for the graphics controller. The device features both EN and active-low EN inputs, accepting active-high or active-low enable inputs. The device also switches and current limits the 5V supply to a VGA connector or monitor. The RED, GRN, and BLU terminals protect graphics controller outputs against electrostatic discharge (ESD) events. All eight outputs and active-low EN have high-level ESD protection. The MAX14895E is specified over the extended -40°C to +85°C temperature range and is available in a 16-pin, 3mm x 3mm TQFN package with exposed pad.

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## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Enhanced VGA Port Protector |
| B. Process: | S45 |
| C. Number of Device Transistors: | 1434 |
| D. Fabrication Location: | California, Texas or Japan |
| E. Assembly Location: | Taiwan, China, Thailand |
| F. Date of Initial Production: | March 25, 2011 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 16-pin TQFN 3x3 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-4458 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 64°C/W |
| K. Single Layer Theta Jc: | 6.9°C/W |
| L. Multi Layer Theta Ja: | 48°C/W |
| M. Multi Layer Theta Jc: | 6.9°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 46X46 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1 = 0.5 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1 = 0.45 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

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## V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 78 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.1 \times 10^{-9}$
$\lambda$ = 14.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.13 @ 25C and 2.31 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TZ1ZAQ001B, D/A 1103)

The AK23 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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**Table 1**

Reliability Evaluation Test Results

**MAX14895EETE+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 78 | 0 | TZ1ZAQ001B, D/C 1103 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

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